

IRAC Test Report
Gallium Doped Silicon Band II
READ NOISE AND DARK CURRENT

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SUMMARY

A direct readout (DRO) infrared detector array, a candidate for the Space Infrared Telescope Facility (SIRTF) Infrared Array Camera (IRAC), has been tested with a readout system built at the Goddard Space Flight Center. The array, developed by Santa Barbara Research Corporation (SBRC) for different applications, has a detector surface of gallium doped silicon, bump bonded to a 58 X 62 pixel MOSFET multiplexer on a separate chip. Although this chip and system do not meet all the SIRTF requirements, the critically important read noise is within a factor of 3 of the requirement. Significant accomplishments of this study include:

1. Development of a low noise correlated-double-sampling readout system with a readout noise of 127 to 164 electrons, (based on the detector integrator capacitance of 0.1 pF),
2. Measurement of the readout noise of the detector itself, ranging from 123 to 214 electrons with bias only (best to worst pixel), and 256 to 424 electrons with full clocking in normal operation, at 5.4 K where dark current is small; 30% smaller read noises are obtained at a temperature of 15 K;*
3. Measurement of the dark current versus temperature, showing the presence of a temperature independent dark current as well as the expected activation energy curve,
4. Measurement of the spatial dependence of dark current, showing unexpected strong differences between pixels and suggesting localized sources,
5. Measurement of the detector/MUX photoelectric gain versus temperature, showing a doubling from 6 to 16 K,
6. Measurement of the multiplexer electrical transfer function, showing the usable range and significant nonlinear behavior,
7. Measurement of the detector response versus integration time, showing significant nonlinear behavior for large signals, well below the saturation level,
8. Discovery of low frequency drifts in the detector and warm electronics, requiring further stabilization efforts,
9. Modeling of the read noise in terms of the MOSFET noise ($1/f$, with 11 microvolts/root Hz at 10 Hz), and preamp noise characteristics,
10. Measurement of the detector noise versus the temperature of a nearby blackbody source,
11. Discovery of unexpected dependences, including variation of the DRO offset voltage with integration time and with temperature,
12. Measurement of the temperature gradient across the mounting, (less than 0.3 K), and thermal response to applied power,
13. Measurement of the required power dissipation in the array,
14. Development of a custom computer interface and suitable software for collection, analysis, and display of the detector data,
15. Development of a test cryostat containing temperature control devices, filtered cables and protective resistors, and a temperature controlled internal IR source.

A number of areas for additional work remain. These include:

1. Temperature stability requirements for the detector and MUX, and possible thermal sources of excess readout noise,*
 2. Studies of additional MOSFET noise parameters, since the MOSFETs in this MUX are not individually accessible.
 3. Improvements in warm electronics to reduce noise, drift, and thermal instabilities, such as a higher resolution (16 bit) analog to digital converter, alterations to the preamplifier, and studies of the clocking signals,
 4. Additional optimization studies regarding temperature and bias, and their effects on dark current, readout noise, and electronic and photo gain,
 5. Optical imaging tests for photometric linearity, spatial resolution, crosstalk, etc.,
 6. Studies of additional detector chips to investigate device dependences and reproducibility of this technology.
- Detailed discussions of these results and areas of future work are contained in the body of this report.

* Very recent results using low noise bias supplies indicate a read noise with 0 volts net detector bias of 120 electrons rms at 5 degrees Kelvin, within a factor of 2 of the noise floor for this device.

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INTRODUCTION

The recent emergence of high performance infrared detector array devices has created a revolution in the field of astronomy. The era of scanned single elements is being replaced with the staring focal plane array with many thousands of elements. The combination of large format detectors and high throughput digital processors operating in a workstation environment has created a new tool for scientific investigation. These detector subsystems are being considered for the next generation of instruments such as infrared imaging cameras and infrared spectrographs. Many new instrumentation concepts have been made possible by virtue of the unique properties of array devices. Used in the next generation of space based observatories, such as the Hubble Space Telescope (HST), the Space Infrared Telescope Facility (SIRTF), and the Large Deployable Reflector (LDR), these developments have the potential of greatly enhancing their scientific value.

The advantages that arrays of detectors have for creating images stem from the large number of pixels, the high positional accuracy, stability in position for those pixels, and from the fact that arrays lend themselves to diffraction limited observations. For arrays of detectors with performance comparable to the best single element detectors and used with identical spatial resolution, the advantage of an array over a single detector for a given signal to noise ratio is N times greater than an individual pixel. This is due to the multiplex advantage of N pixels on the scene.

Extensive work has been done in applying infrared array devices to ground based astronomy (1-8). The demonstrated performance of these types of devices, and the emergence of newer structures tailored for space low background applications served as a basis for the Infrared Array Camera (IRAC) proposal for SIRTF. During the SIRTF/IRAC proposal study, a survey of the available technology to date highlighted the direct readout (DRO) technology as the primary SIRTF candidate.

As such, the objective for the current IRAC detector evaluation effort is to determine the performance of existing direct readout array devices in comparison to the limiting performance for a particular detector/multiplexer design, to other array technologies, and to existing single element detector 'systems'. Furthermore, these tests are to be conducted under conditions as near as possible to actual SIRTF operating conditions to firmly establish actual performance capabilities.

BACKGROUND

The SIRTf performance will be driven primarily by the detector performance and the specific science requirements for each instrument. We have established the minimum detector requirements to accomplish the scientific objectives for the IRAC instrument. Table 1 is a list of the projected performance for the IRAC Band II detector which is the focus of our investigation. These performance goals are an order of magnitude improvement in sensitivity over currently available systems.

Table 1. SIRTf/IRAC Band II Focal Plane Performance Goals at Peak Wavelength

Wavelength Range	5-17	micrometer
Peak Wavelength	15	micrometer
Format	64 x 64	
Responsive Quantum Efficiency	0.4	
Photoconductive Gain	0.5	
Responsivity	2.8	A/W
Read Noise	< 100	e rms
Read Noise Limited NEP (rel. 1 sec. integration)	1×10^{-17}	W/ $\sqrt{\text{Hz}}$
Dark Current	< 100	e/sec per pixel
Dark Current Limited NEP	1×10^{-18}	W/ $\sqrt{\text{Hz}}$
Focal Plane Power Dissipation (@ 1 frame/sec. readout)	< 3	mW

The expected sensitivity for this type of array detector can be determined from a consideration of the various noise sources, and the detector performance. The array noise equivalent power (NEP) is defined as the incident radiation power necessary to produce a signal to noise ratio (SNR) of unity in a unit noise bandwidth:

$$\text{NEP} = (2/t)^{1/2} \cdot (hc/\lambda) \cdot (N_t)/\text{QE} [\text{W}/\sqrt{\text{Hz}}]$$

where, N_t = total rms number of electrons
 QE = quantum efficiency
 h = Planck's constant
 c = speed of light
 λ = wavelength
 t = integration time

The total charge noise referred to the detector input is fundamentally limited by the background photon flux level during the integration time, the detector dark current during the integration time, the integrator reset noise, cryogenic MOSFET preamplifier noise, and the system noise (by which we mean preamp and sampling system):

$$N_t^2 = N_b^2 + N_{dc}^2 + QkTC^2 + Q_{fet}^2 + Q_{sys}^2 [\text{e rms}]$$

N_b = eq. input background noise
 $= [a \text{ QE } P \text{ Ad } t \text{ tr}]^{1/2}$
 $a = 1 \text{ (PV)} ; 2 \text{ (PC)}$
 P = photon irradiance $\text{p}/(\text{s cm}^2)$
 Ad = detector area cm^2
 tr = optic transmission

N_{dc} = eq. input dark current noise
 $= [(a J_{dc} A_d t) / (q PG)]^{1/2}$
 J_{dc} = meas. dark current density (A/cm²)
 q = electron charge
 PG = photoconductive gain

Q_{kTc} = eq. input reset noise
 $= [(b N_{kTC}) / (PG)^2]^{1/2}$
 $b = 0$ (CDS filtering)
 $= 2$ (delta reset)
 N_{kTC} = reset noise, see array section

Q_{fet} = eq. input transistor noise
 $= [(d N_{fet}) / (PG)^2]^{1/2}$
 N_{fet} = see MOSFET noise section
 $d = 2$ (digital algorithm)
 $= 1$ (delta reset)

Q_{sys} = eq. input system noise
 $= [(d N_{sys}) / (PG)^2]^{1/2}$
 N_{sys} = Equivalent input
 quadrature sum of system
 noise sources

This reduces to the familiar background limited NEP expression in the absence of dark current, reset, transistor, or system noise. As the integration time t is varied, the background and dark current contributions are constant whereas the reset (kTC) and MOSFET transistor and system contributions taken together as read noise are proportional to $(1/t)^{1/2}$. The time t where the background and dark current contributions equals the reset noise contribution is the critical integration time below which the system is read noise limited and above which the system is shot noise limited.

The impact of the read noise and dark current on the system performance can best be understood by looking at the improvement in the signal to noise ratio (SNR) of an on-chip integration with respect to the time of that integration. The improvement in SNR verses integration time for an arbitrary source SNR of 60 can be seen in Figure 1. For short integration times the noise on the integrated photo current is less than the read noise and the SNR improves linearly in time. At the critical integration time the two noise components are equal, and for greater integration times the SNR improves as the square root of the integration time. In going from a read noise of 320 e rms to 100 e rms the critical time shifts by a ratio of the square of the ratio of read noises. Therefore, in reducing the read noise the background limit can be reached sooner.

The shot noise from the detector dark current will set the remaining boundary on the background limited NEP. As signal and background photon fluxes are lowered the detector dark current component will become the dominant term. In the absence of any photon flux a critical integration time is reached when the dark current shot noise equals the read noise. This dark current 'background' combined with the read noise defines the array limiting NEP.

The importance of the array read noise and dark current noise are evident and, consequently, the determination of the array read noise and dark current were the major thrust of this study.

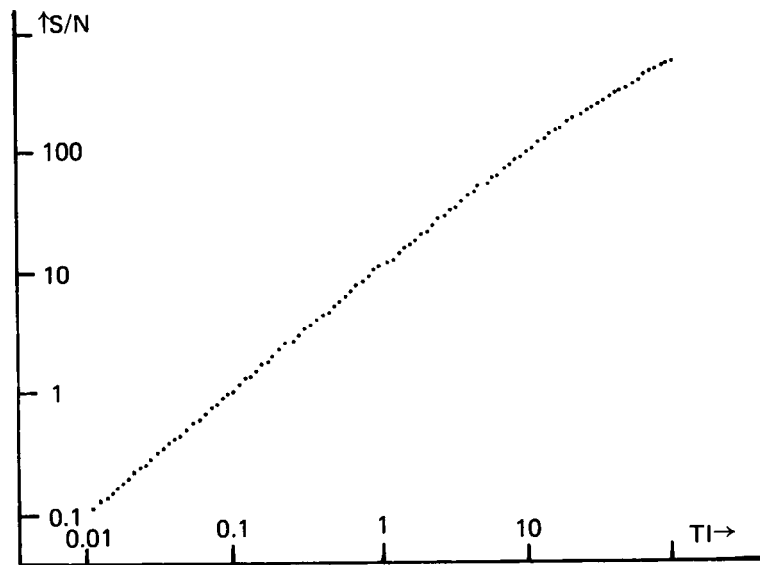
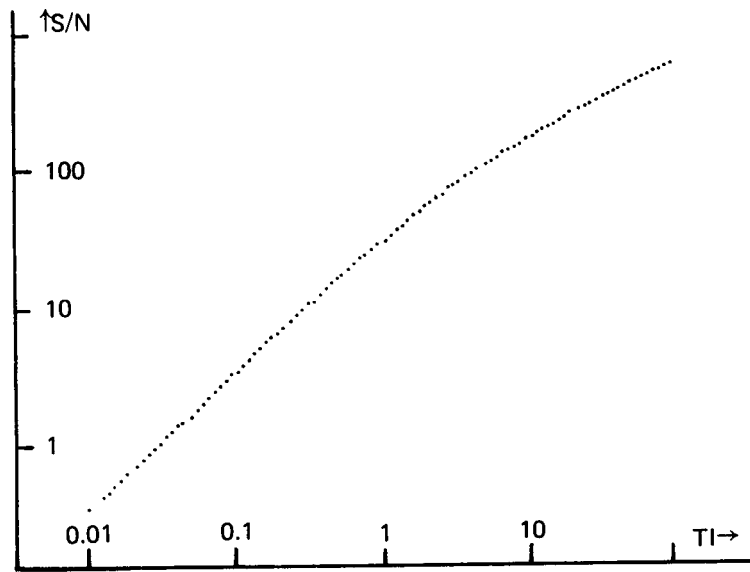


Figure 1. Signal to Noise Improvement With Integration Time.

x axis Integration Time (sec)

y axis Signal to Noise ratio (S/N)

Top Figure: $S/N = 60$ $N_{read} = 100$ e rms

Bottom Figure: $S/N = 60$ $N_{read} = 320$ e rms

ARRAY

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The array under investigation is a Hughes Carlsbad Research Center (CRC)/Santa Barbara Research Center (SBRC) hybrid infrared array provided to GSFC for evaluation. The hybrid array consists of a detector substrate indium bump bonded to a silicon DRO multiplexer. A typical hybrid array mounted in a 68 leadless chip carrier is shown in Figure 2. The advantage of the 'hybrid' technology is that both the detector material and its processing, and the multiplexer and its processing can be independently optimized. The detector material under consideration for the IRAC Band II is gallium doped silicon (Si:Ga). The multiplexer under investigation is a model CRC 228 direct readout NMOS integrated circuit. Photographs of the DRO array with and without the detector substrate are shown in Figures 3 and 4. Visible in the center is the 58 x 62 array of indium bumps. The bonding pads to the multiplexer are visible along the top and bottom.

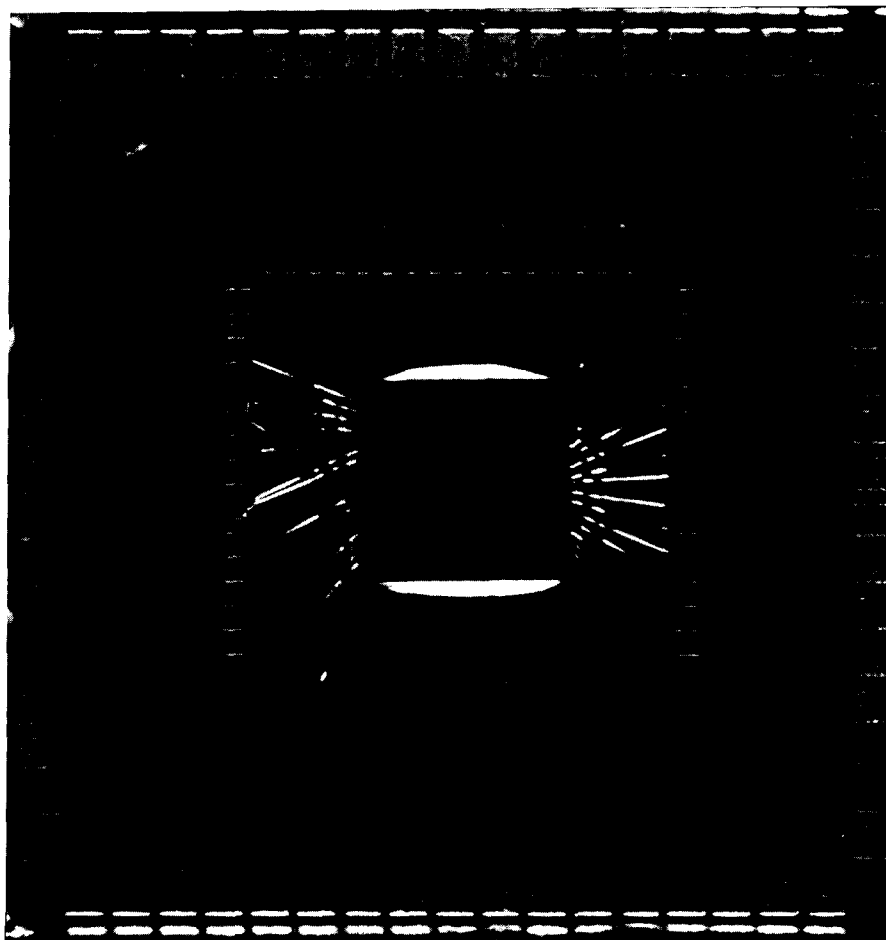


Figure 2. DRO Array in Leadless Package.

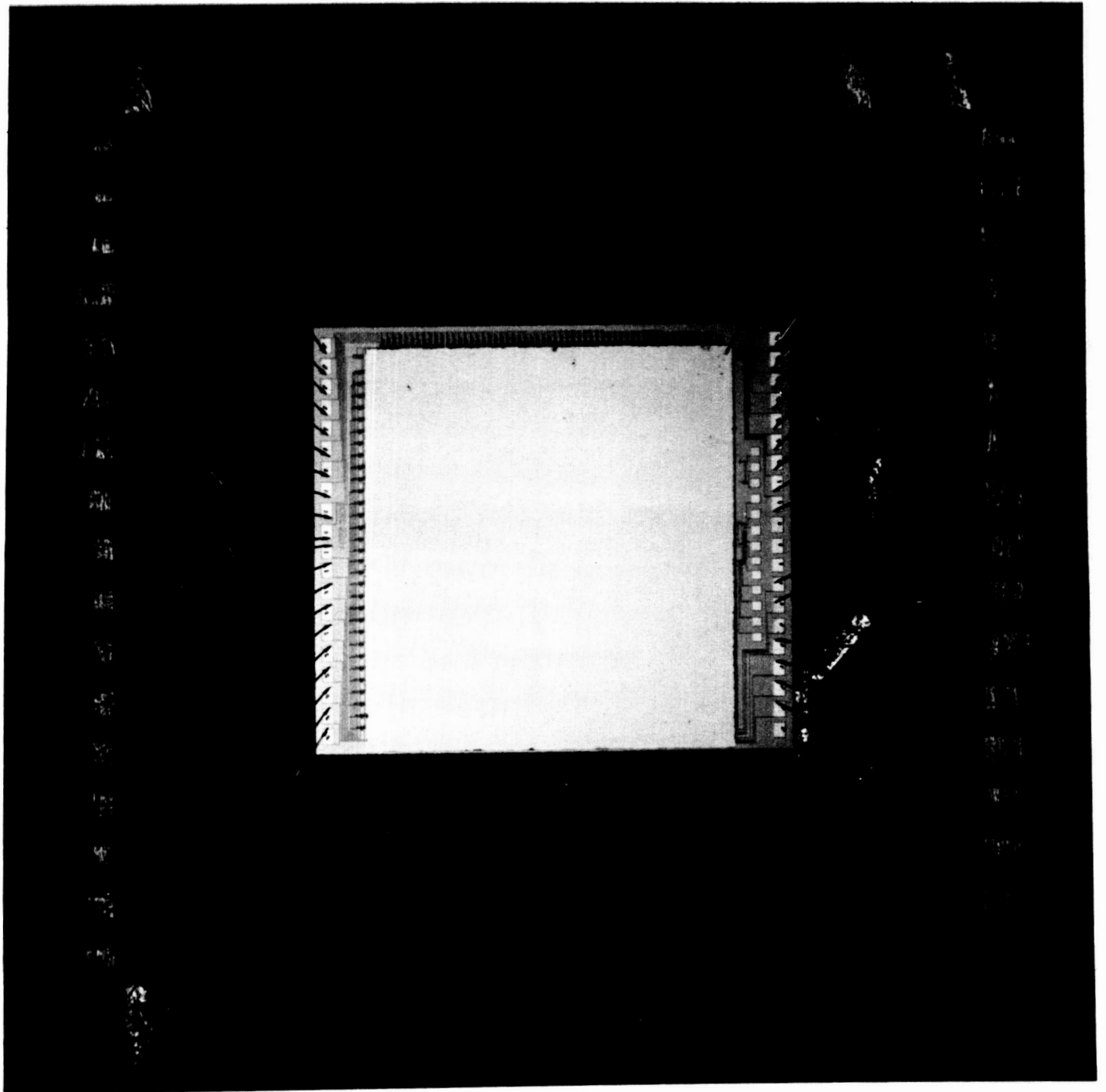


Figure 3. Detail of DRO with Detector Substrate.
(Photo courtesy of SBRC)

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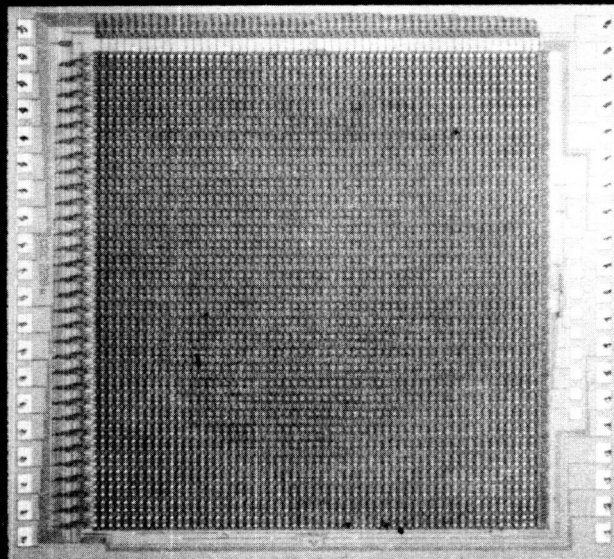


Figure 4. Detail of DRO with Detector Substrate Removed.
(Photo courtesy of SBRC)

The characteristics of the hybrid array and focal plane module are outlined in Table 2. The values used in the table are explained in the text.

Table 2. Focal Plane Characteristics

Detector Material	Si:Ga	
Wavelength Range	3-17	micrometer
Peak Wavelength	15	micrometer
Ionization Energy	0.0827	eV
Dopant Concentration	$5-6 \times 10^{16}$	$\#/cm^3$
Format	58 x 62	
Pixel Size	75 x 75	micrometer
Pixel Spacing	75 x 75	micrometer
Pixel Active Area (Ad)	5.6×10^{-5}	cm^2
Detector Thickness	500	micrometers
Multiplexer	CRC-228	
Format	3 of 7 row decoder 3 of 7 column decoder	
Source Resistor (Rs)	100K	Ohm
DRO Cryoamp Gain (Gdro)	0.7	
Sense Node Cap. (Cn)	0.1	pF
Electronic Response (Se)	1.12	microvolt/electron
Saturation Signal	2×10^6	electrons
Array Power Dissipation	3	milliwatts
Temperature Monitor	Germanium Resistance Thermometer	
Heater (Thin Film)	1000	Ohm

Detector bias is applied to a transparent implanted contact on one surface of the detector substrate. The opposite face of the detector substrate is patterned with an array of indium bump bonds at the pixel unit cell period in a 58 x 62 format. The pixels are formed by the electric field patterns within the detector substrate between the common bias electrode and the indium bumps. In effect, an image is formed by the absorption of photons in a continuous piece of material. Photo current generated in the detector pixels is integrated on the node capacitance of the DRO readout multiplexer at the indium bump contact.

The integrated photo charge is buffered by a cryogenic preamplifier. This amplifier is formed by cascading two common drain amplifiers, where the first is in the unit cell and the second is common to half of the pixels in the array. There is, therefore, a unique amplifier gain for each detector. The array is read out through the selection of unit cells in a sequence determined by the row and column address codes and through the readout and reset clock sequence.

Unit Cell Performance

A simplified description of the CRC 228 circuit function is as follows. The schematic of a unit cell and the signal as seen at the output is shown in Figure 5. Transistors Q9 through Q12 form a resettable three input column select gate and transistors Q13 through Q16 form a resettable three input row select gate. A particular unit cell is selected by a unique combination of three of seven lines for both the column and the row. When a particular unit cell is selected Q5 connects the drain supply to the unit cell amplifier formed by Q1 and Q2. Transistor Q1 is the first amplifier from the detector, where the gate capacitance is the dominant component to the sense node capacitance Cn. Transistor Q2 is biased as an active load device for the unit cell amplifier. Transistor Q7 connects the output to the even array driver formed by Q3 and a cold 100K ohm source resistor. The buffered and multiplexed output from the even array pixels is available from the array driver (out even). A mirror of the above described circuit is connected to the odd pixels. For any address selected both an even and an odd pixel are available from the array. After an integration the sense node is reset by the reset switch Q4. During the unit cell selection, transistors Q6 and Q8 were activated to allow the reset clock and the reset potential to access the unit cell.

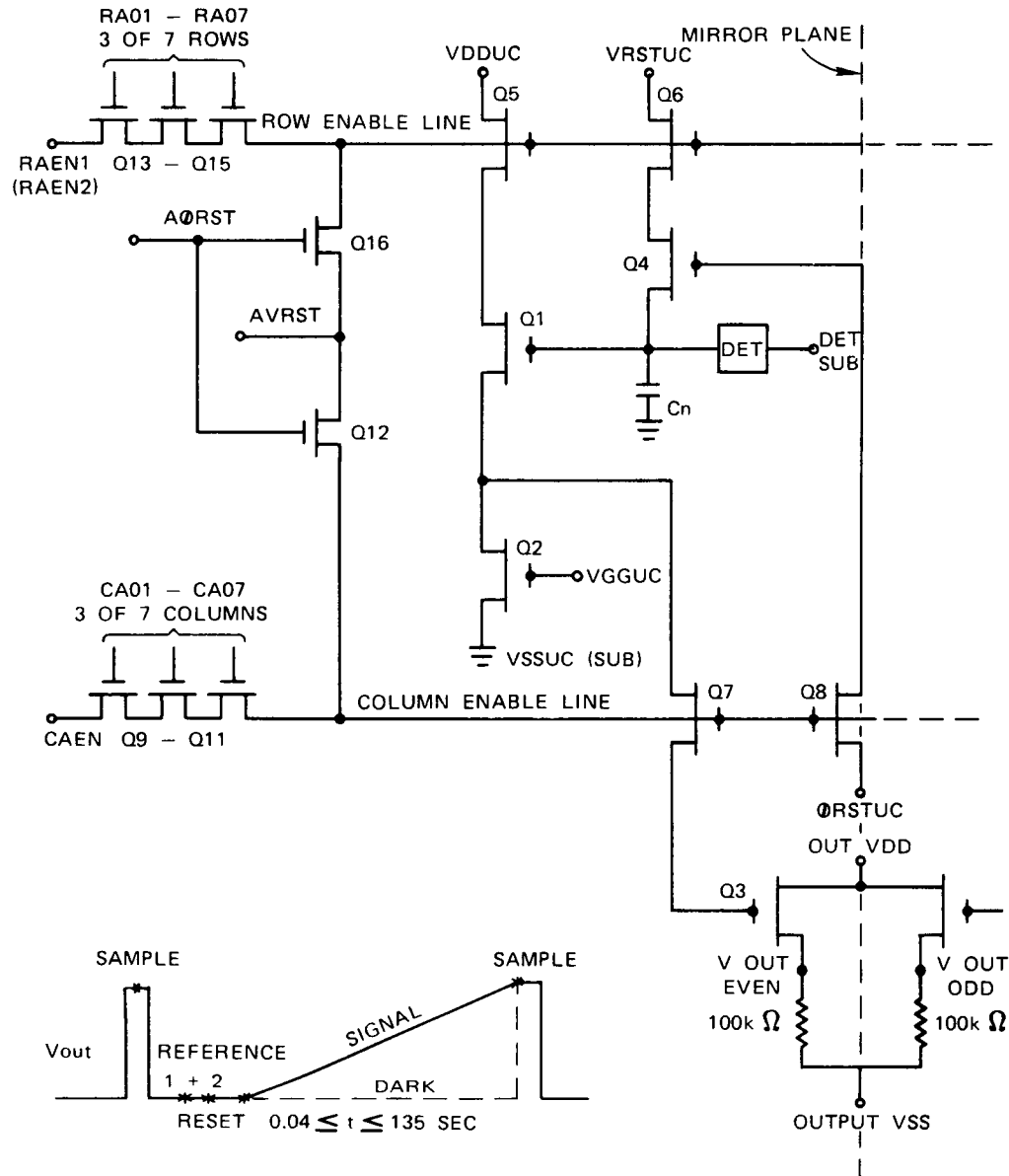


Figure 5. DRO Address Decoder, Unit Cell and Output Driver Schematic.

The output of the array, with the times scales greatly exaggerated, is shown in Figure 5 and a detail during the readout time is shown in Figure 6. The DRO DC output level is determined by the unit cell and output driver threshold voltages at their operating currents. The AC component is due to the displacement pulse from the reset clock, the address valid clock, and the integrated signal. The reset pulse duration is fixed and typically 60 microseconds. The reset pulse width is determined by the filter sampling interval discussed in the electronics section. The pixel readout rate is adjustable from 300 microseconds to 1 second per pixel. The integration time depends on the subarray size and the pixel readout rate. For these tests the subarray size was 16 x 16 pixels, therefore, the integration time was adjustable from 0.04 seconds to 135 seconds. The solid line from the RESET level to the SAMPLE level is a trace of the output of a single addressed unit cell during the integration time in the presence of a signal flux. With the scanner activated the

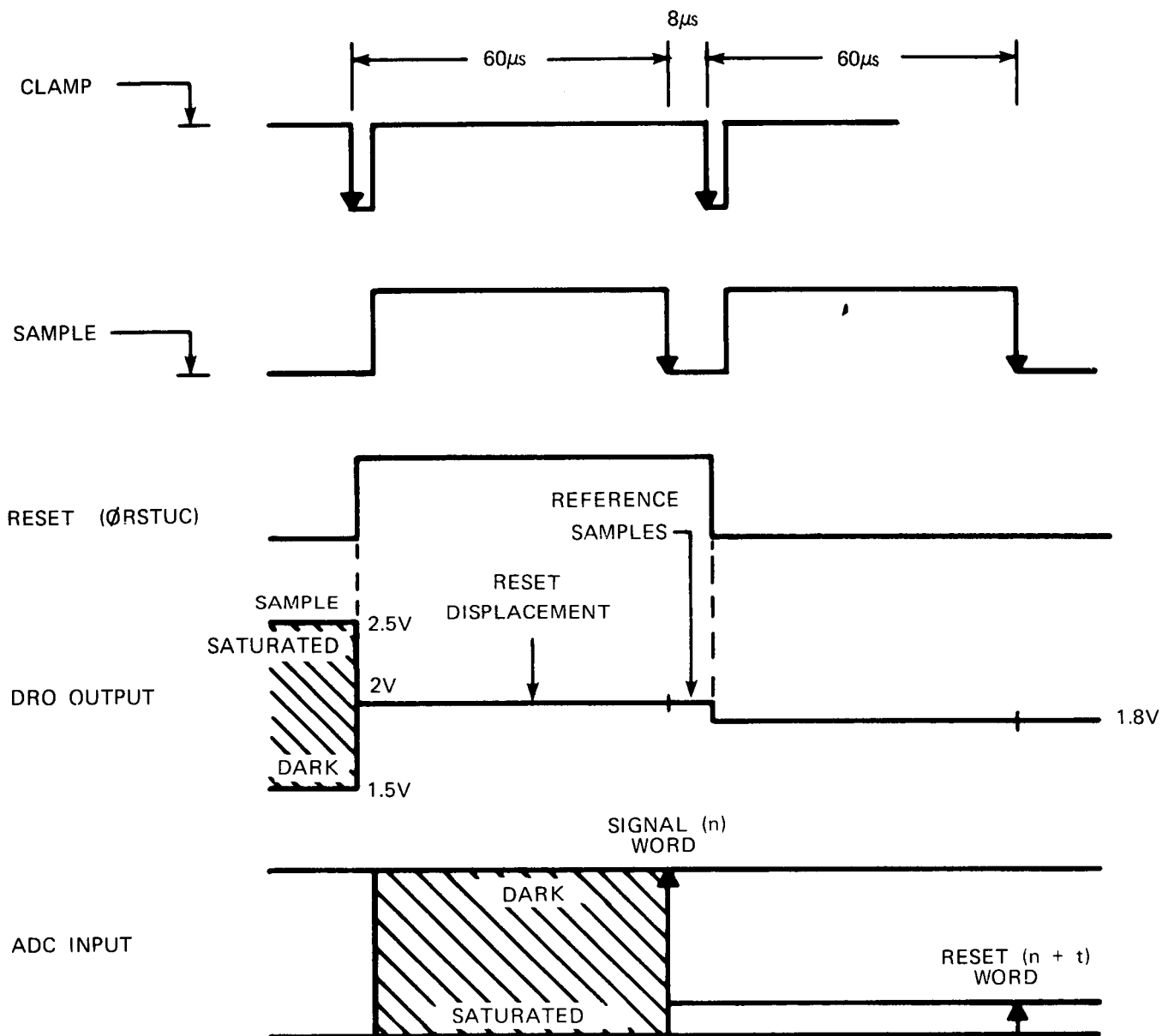


Figure 6. Sketch of Array Signal From Analog Processing Chain.
Refer to Figure 20 for the circuit diagram.

value of the selected pixel would be multiplexed with 1797 other pixels in a uniform time multiplexed manner. The dotted line is the response from the same selected pixel when multiplexed. There are 1797 individual pixel sample values uniformly distributed within the time interval from RESET to SAMPLE.

A detailed sketch of the array output signals at various points in the signal processing chain during a unit cell readout is seen in Figure 6. The readout mode is a form of correlated sampling and is discussed in detail in the section on electronics. The top two traces are the analog processor clamp and sample waveforms. The third trace is the unit cell reset pulse. The next trace is the array direct output. The reset displacement pulse transition from on to off at the output is shown. The bottom trace is the analog to digital converter input.

The unit cell reset pulse is coupled into the output due to the finite parasitic coupling capacitance between the reset clock line and the sense node. Assuming a simple parallel plate capacitor model for the parasitic coupling and minimum geometry devices the estimated parasitic capacitance is:

$$C1 = \epsilon_r \epsilon_o A_p / t_{ox} \\ = 7 \text{ fF}$$

Where:

$$\begin{aligned} \epsilon_r &= \text{relative dielectric constant for SiO}_2 \\ &= 4 \\ \epsilon_o &= \text{permittivity of free space} \\ &= 8.85 \times 10^{-14} \text{ F/cm} \\ t_{ox} &= \text{oxide thickness} \\ &= 1000 \text{ angstrom} \\ A_p &= \text{area of capacitor} \\ &= 2 \times 10^{-7} \text{ cm}^2 \end{aligned}$$

From the input reset pulse amplitude, the estimate of the clock coupling capacitance, and the sense node capacitance, the reset clock displacement is estimated as:

$$V_p = V_{cl} C1 / (C1 + C_n) \\ = 0.320 \text{ volts}$$

Where:

$$\begin{aligned} C_n &= \text{sense node capacitance} \\ &= 0.1 \text{ pF} \\ V_{cl} &= \text{reset clock amplitude} \\ &= 5 \text{ volts} \\ C1 &= 7 \text{ fF} \end{aligned}$$

This compares with a measured reset displacement of 0.2 volts.

The array preamplifier is connected in a cascaded common drain configuration. In effect, it converts the signal charge injected onto the sense node gate capacitance C_n in the unit cell into an equivalent voltage change at the output driver. The net sense node capacitance at the gate of the unit cell amplifier and the array preamplifier transfer function determine the array sensitivity per electron charge.

Considering the output driver first, where the transistor drain to source resistance is larger than the preamplifier source resistance, the voltage transfer function is:

$$A_v = g_m R_s / (1 + g_m R_s)$$

Where:

$$\begin{aligned} g_m &= \text{transistor transconductance at cryogenic temp.} \\ R_s &= \text{cold source resistor} \end{aligned}$$

For large source resistances and large transconductances the voltage gain approaches unity. For the CRC 228 device the cryogenic transconductance is about 620 micromhos at a drain current of 130 microamps and the source resistance is 100K ohms resulting in a gain in the preamplifier of about 0.98.

The unit cell amplifier is also a common drain amplifier but uses an integrated circuit source load transistor Q2. This transistor is biased as a constant current source and therefore approximates an ideal load device. Back gate bias effects in the integrated circuit and the minimum geometry of the unit cell amplifier reduce the actual gain of the unit cell amplifier. The composite gain of the array preamplifier is the product of the unit cell amplifier and the output drain amplifier.

The electrical transfer function for a typical unit cell is plotted in Figure 7. This data was taken by setting the detector bias to the reset potential (V_{rst}), looking at the array output (source lead of Q3) and varying V_{rst} in steps. Evident in this plot are the turn on, sub threshold, and saturation in the cryogenic preamplifier. The region from $3.0 < V_{rst} <$

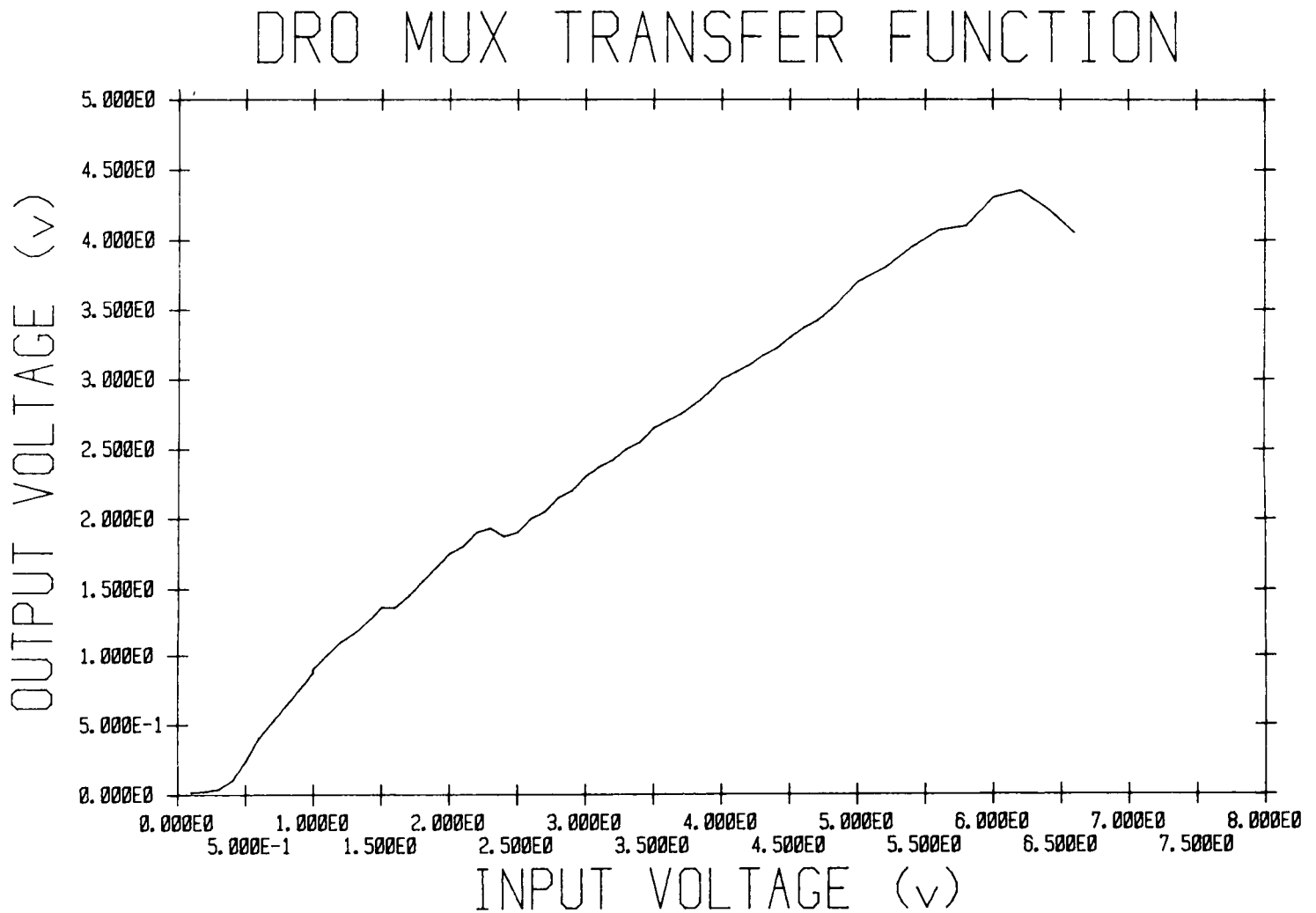


Figure 7. DRO Array Electrical Transfer Function.

The array direct output versus reset potential input (V_{rst}) swept from 0 to 7 volts. The focal plane temperature was 5.76 kelvin, the array frame rate was 70 f/s, and the net detector bias was zero.

6.0 volts is the linear operating region for the DRO cryogenic preamplifier. The saturation at 4.4 volts is due to this preamplifier and sets a maximum integrated input level at about 6 volts and the saturation signal level to 2×10^6 e. To operate the array in the linear region the reset potential V_{rst} was set to 3.0 volts. Under these operating conditions the gain was measured to be 0.7 as compared with the expected composite gain of 0.96. This result is in a reasonable range for devices operated at cryogenic temperatures where detailed models of the transistors are non-existent.

The net sense node capacitance at the gate of the unit cell amplifier determines the unit cell sensitivity per electron charge. For the array tested the node capacitance is the sum of the unit cell amplifier intrinsic gate capacitance (0.08 pF), the indium bump bond capacitance (0.01 pF), and the detector capacitance (0.01 pF). The total estimated node capacitance is 0.1 picofarads. Therefore, the unit cell charge sensitivity is:

$$\begin{aligned}
 S_e &= (q * G_{dro}) / (C_n) \\
 &= 1.12 \text{ microvolt/electron}
 \end{aligned}$$

Where:

$$\begin{aligned} q &= \text{electron charge} \\ G_{dro} &= \text{total array preamplifier gain} \\ C_n &= \text{sense node capacitance} \end{aligned}$$

This array preamplifier buffers the detector from the warm electronics and provides an impedance transformation from the high detector impedance to the moderately low system impedance. In the process of interfacing the detector to the downstream electronics this amplifier inevitably adds additional noise and since the gain is less than one the effects of downstream electronics noise must be considered in the noise analysis. The rms noise of this cryogenic MOSFET preamplifier, the warm preamplifier and the system electronics over the system information bandwidth combined with the noise associated with the reset of the node capacitance and any quantization error determines the array readout noise. For the array running at 6 kelvin, the value in electrons rms of the reset noise component associated with the node capacitance C_n is:

$$\begin{aligned} N_{kTC} &= (kTC_n/q)^{1/2} \\ &= 18 \text{ e- rms} \end{aligned}$$

Where

$$\begin{aligned} k &= \text{Boltzmann's constant in electron volts} \\ &= 8.62 \times 10^{-5} \text{ eV/K} \end{aligned}$$

For array noise comparisons the important parameter to consider is the preamplifier rms noise charge or the product of the rms noise voltage and the effective input capacitance. The choice of the MOS transistors over JFET devices is in the potentially lower sense capacitance, the ability to operate at the focal plane temperature, and the ability to manufacture large arrays of devices using large scale integrated circuit techniques. This has important implications for focal plane arrays with large numbers of elements.

The noise in a FET device is best described as the superposition of a broadband component determined by the channel conductance and a $1/f$ component. For the unit cell transistor geometry (with an assumed transconductance of 12 micromhos) the worst case broadband component at 6K is:

$$\begin{aligned} e_n/\text{root BW} &= (8kTq/3g_m)^{1/2} \\ &= 4.2 \text{ nV}/\sqrt{\text{Hz}} \end{aligned}$$

Data on the noise spectral density for the individual devices in the CRC 228 are not available. However, a model assuming $1/f$ noise and a value of 2 microvolt/root Hz @ 10 Hz was used based on the noise of test devices. The $1/f$ noise corner frequency is where the $1/f$ component and the thermal component intercept. Using the broadband floor and the $1/f$ model the corner frequency is:

$$\begin{aligned} F_n &= f_1 * (e_{n1}/e_{n2})^2 \\ &= 2.27 \text{ MHz} \end{aligned}$$

Where:

$$\begin{aligned} f_1 &= 10 \text{ Hz} \\ e_{n1} &= 2000 \text{ nV}/\sqrt{\text{Hz}} \\ e_{n2} &= 4.2 \text{ nV}/\sqrt{\text{Hz}} \end{aligned}$$

The net read noise referred to the input sense node due to the array preamplifier is the quadrature sum of the noise contributions of the individual transistors weighted by the gains between the source and the input. Referring to Figure 5, the charge detected on the node capacitance C_n is amplified by the common drain amplifier formed by Q1 and Q2, transmitted by transistor Q7 and amplified by transistor Q3. The net input noise is then:

$$ent = (en1^2 + en2^2 + (en3^2)/Gu + (en7^2)/Gu)^{1/2}$$

Since the unit cell gain is nearly unity, and the noise in each transistor is assumed equal and the same as the test devices, the net input noise is:

$$\begin{aligned} ent &= (4 * en^2)^{1/2} \\ &= 2 * en \end{aligned}$$

The equivalent input charge noise is the integral of the product of the device noise spectral density and the system transfer function. A computation of the DRO cryogenic preamplifier noise with the analog processor is covered in the read noise summary. The equation describing the read noise contribution is:

$$N_{fet} = 1/(Se) \left\{ \int_0^{BW} [2 * en |T(s)|]^2 df \right\}^{1/2}$$

Where:

$$\begin{aligned} T(s) &= \text{analog processor transfer function} \\ BW &= 220 \text{ kHz} \\ Se &= 1.12 \text{ microvolt/electron} \end{aligned}$$

The cryogenic preamplifier output impedance is approximated by the parallel combination of the common drain channel resistance, the inverse of the transistor transconductance, and the source load resistance.

$$Ro = (Rs * rds)/(rds + gm rds Rs + Rs)$$

For the CRC 228 where the transistor drain-source resistance is very large, this reduces to:

$$Ro = Rs/(1 + gm Rs)$$

A measured output resistance of 1600 ohms for a cold source resistance of 100K ohms and a drain-source bias current of 130 microamps imply a cryogenic transconductance gm of 620 micromhos for the DRO output transistors.

A pin assignment diagram of the Si:Ga DRO array is shown in Figure 8 and the DRO DC bias was set to the values listed in Table 3.

Table 3. Optimum DRO Operating Biases @ 5.7 Kelvin.

Name	Volts	Description
Vdduc	6.0	Unit cell drain bias
Vgguc	0.7	Unit cell active load gate bias
Vssuc	0.0	Unit cell source (grounded)
Vrst	3.0	Unit cell reset potential
Vod	15.0	Output driver drain bias
Vos	0.0	Output driver source grounded
ORST	5.0	Reset pulse amplitude
AORST	5.0	Column and row reset clock
AVRST	0.0	Column and row reset potential
RAE1,RAE2	5.0	Row address enable potential
CAEN	5.0	Column address enable potential
R1-R7	5.0	Row select address amplitude
C1-C7	5.0	Column select address amplitude
GRNGR,GRNGL	0	Guard rings (grounded)
SUB	0	Multiplexer substrate (grounded)

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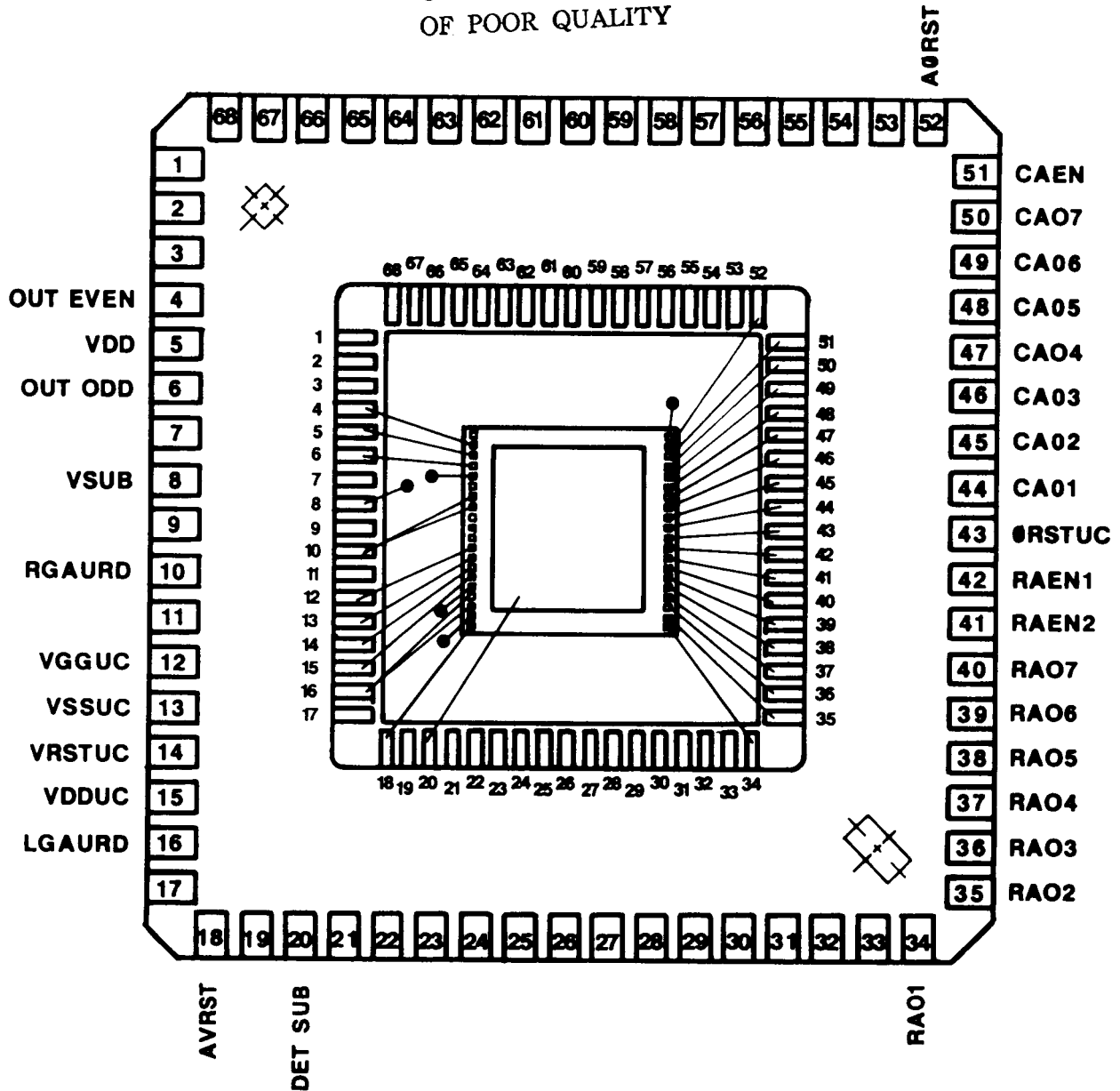


Figure 8. CRC 228 Si:Ga DRO Array Pinout Diagram.

The CRC 228 DRO device pin definitions are shown. Definitions and values for the connections are listed in Table 3. (Sketch courtesy of SBRC)

The response of the array to the various biases was investigated while looking at the output of a unit cell. With all clock amplitudes equal, the threshold clock level necessary to operate the array at 5.7 kelvin was 3.6 volts. For unit cell drain voltages less than 3.0 volts, the saturation level and linear range are degraded. The unit cell gate bias, Vgguc, determined the speed in the DRO cryogenic preamplifier as shown in Figure 9. The traces show the time required to track the reset of the sense node. For Vgguc equal to 0.7 volts the reset response time is 50 microseconds, for voltages less than 0.7 volts the response is significantly slower. The operating bias voltages used for performance testing were selected because they allowed operation over a broad range of operating temperatures and integration times without the need to make adjustments.

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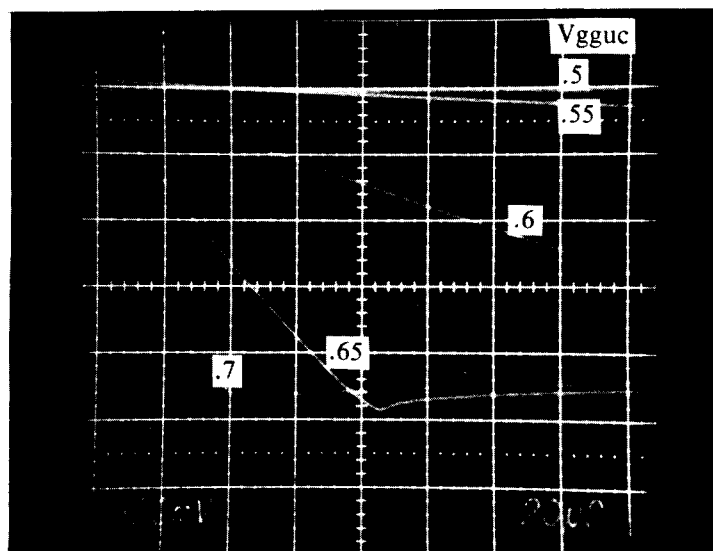


Figure 9. Unit Cell Load Device Bias.

The reset level condition is seen in this photograph. The vertical sensitivity is 500 mV/div and the horizontal resolution is 20 microseconds/div. The steps range from 0.5 to 0.7 volts in 0.05 volt steps. The response falltime was minimized for Vgguc values greater than 0.7 volts. For bias values less than 0.65 volts the reset response time was excessively long.

The focal plane array power dissipation is composed of the dissipation in the two array driver amplifiers and loads, the unit cell amplifier and active load, the cryogenic NMOS multiplexer in the DRO, and the focal plane heater. The dissipation in each of the driver amplifiers is:

$$\begin{aligned} P_{diss} &= V_{od} * (V_{dc}/R_s) \\ &= 0.26 \text{ mW} \end{aligned}$$

The DC output voltage (Vdc) is 2.00 volts set by Vrst and the operating threshold voltages of Q1 and Q3 including back gate bias effects. The driver source resistance is 100K ohms. The driver amplifier power for both channels is, therefore, about 0.52 mW.

The dissipation in the unit cell amplifier and in the DRO multiplexer scanner was determined by measuring the total power and subtracting the calculated driver amplifier power. The power dissipation has been measured by the substitution method. The temperature of the focal plane is recorded at an operating frame rate, the array biases are removed and the focal plane heater is increased to give the same temperature. The dc voltage and current in the heater then give the equivalent total power dissipated. By this method the total focal plane power has been measured as 2.51 mW for a worst case frame rate of 70 f/s. The average power dissipated in the unit cell amplifier and DRO multiplexer scanner at 70 f/s is, therefore, 2 mW.

DEWAR

The dewar is an IR Labs model HD-3 with a lengthened case (Figure 10). This dewar has a 1.2 liter liquid helium capacity and a 0.8 liter liquid nitrogen reservoir. The basic dewar was modified to include low thermal conductance stiffeners between reservoirs, cold optical table, helium radiation shield, an eight position cryogenic intermittent filter wheel mechanism, a lens barrel, an internal infrared reference source, a focal plane mount and an electrical interface board.

All assembly was with 0.005" indium gasket material between surfaces to minimize the cool down time which is typically 4 hours to operating temperature.

The electrical interface (Figure 11) is provided by four 16 pin integrated circuit sockets on a printed circuit board. To minimize electrical crosstalk and thermal loading, shielded stainless steel coax cable connect the cold interface board to two 32 pin hermetic connectors in the dewar top plate. These cables are thermally strapped to the helium, nitrogen, and shell surfaces of the dewar. The DRO package is wired to the interface board with teflon coated 0.005" manganin wire and integrated circuit plugs.

The DRO 68 pad leadless package is mounted into an AMP leadless socket mounted on the detector interface printed circuit board (Figure 12). All of the leads are current limited by 1000 ohm series limiting resistors and 300K ohm static discharge resistors. The DRO array is held against the cantilevered socket pads by a baffled snout limiting the array field of view to the filter wheel and internal reference source along the optical axis (Figure 13). This arrangement limits the acceptance angle of any stray light present within the helium box surrounding the array as well as spring loads the device in the socket. A detail of the back of the DRO interface printed on the circuit board (Figure 14) shows the location of the calibrated germanium resistance thermometer (GRT) temperature monitor. All unused pads from the array package are tied to the copper ground plane on the interface board to minimize the thermal drop from the array to the sensor.

The detector mount is tied to the cold surface through a thermal resistance formed with a piece of fiberglass printed circuit board 0.0625" thick and two 4-40 stainless screws. The effective thermal resistance is 111 kelvin/watt. A 1000 ohm heater resistor (not shown in Figure 14) is epoxied below the temperature monitor to set the focal plane temperature. The calibrated GRT mounted on the interface printed circuit card described above was used to monitor the focal plane temperature. An independent determination of the detector array substrate temperature indicates less than 0.33 kelvin offset between the temperature monitor and the substrate. With this arrangement the focal plane temperature could be varied from 5.4 - 20 K with about 0 - 100 milliwatts of heater power.

An internal infrared thermal source is mounted on the optical axis of the array (Figure 15). There is a 1N914 diode chip epoxied to the source to monitor the temperature. Calibration curves for the source temperature verses power dissipation are plotted in Figure 16. The source can be set from the bath temperature to above 500 K with power from 0 to 80 milliwatts. The 10% to 90% response time for this source is less than 3 seconds.

In addition to the calibration source, a calibrated background monitor was installed within the cold shield to monitor the background flux.



Figure 10. Liquid Helium Test Dewar.

The upper can is the helium reservoir and the lower the nitrogen reservoir. Also visible are the cold table mechanical and electrical interfaces as well as an optical barrel.

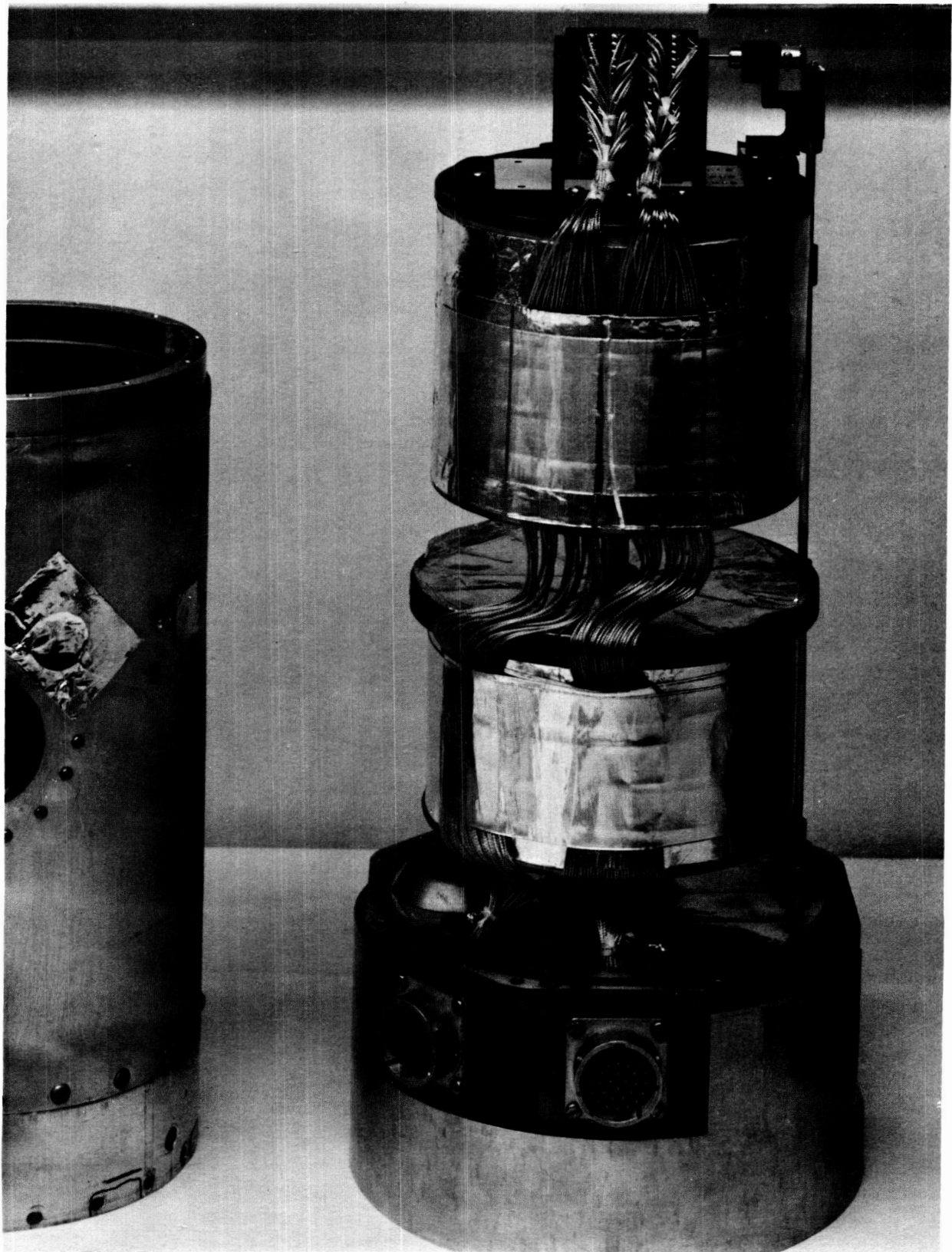


Figure 11. Dewar Electrical Interface.

Visible in this photograph are the 64 stainless steel coaxial cables, the cold termination board, and the hermetic feedthrough connectors for the electrical interface to the array.

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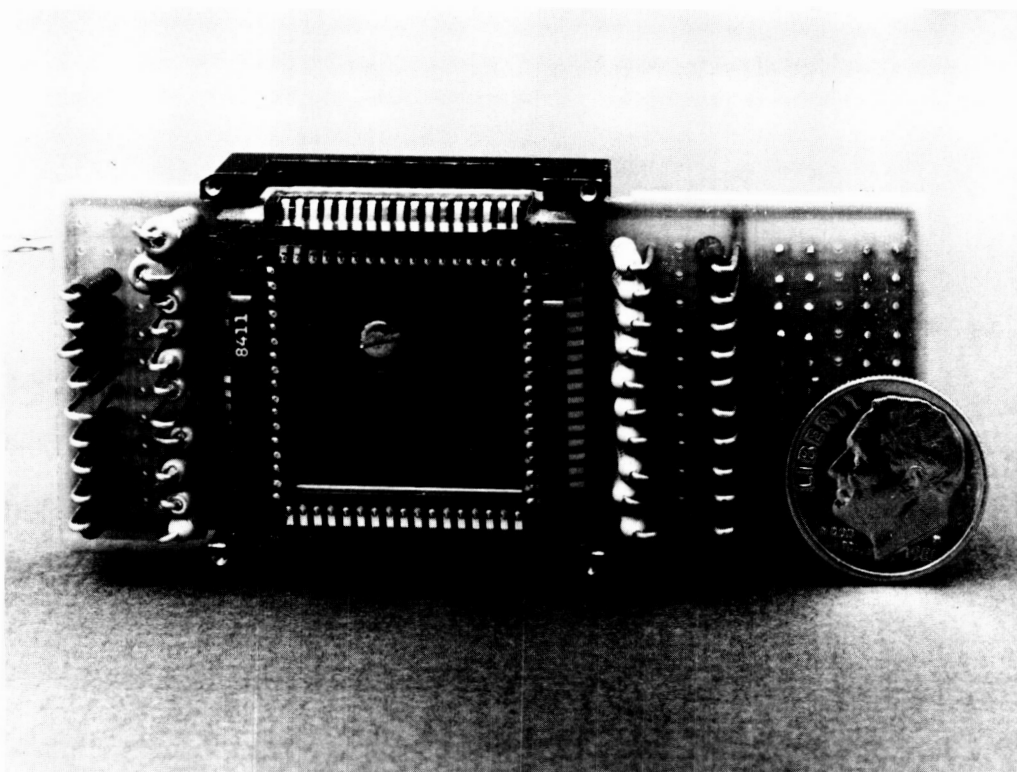


Figure 12. Array Cryogenic Electronic Interface.

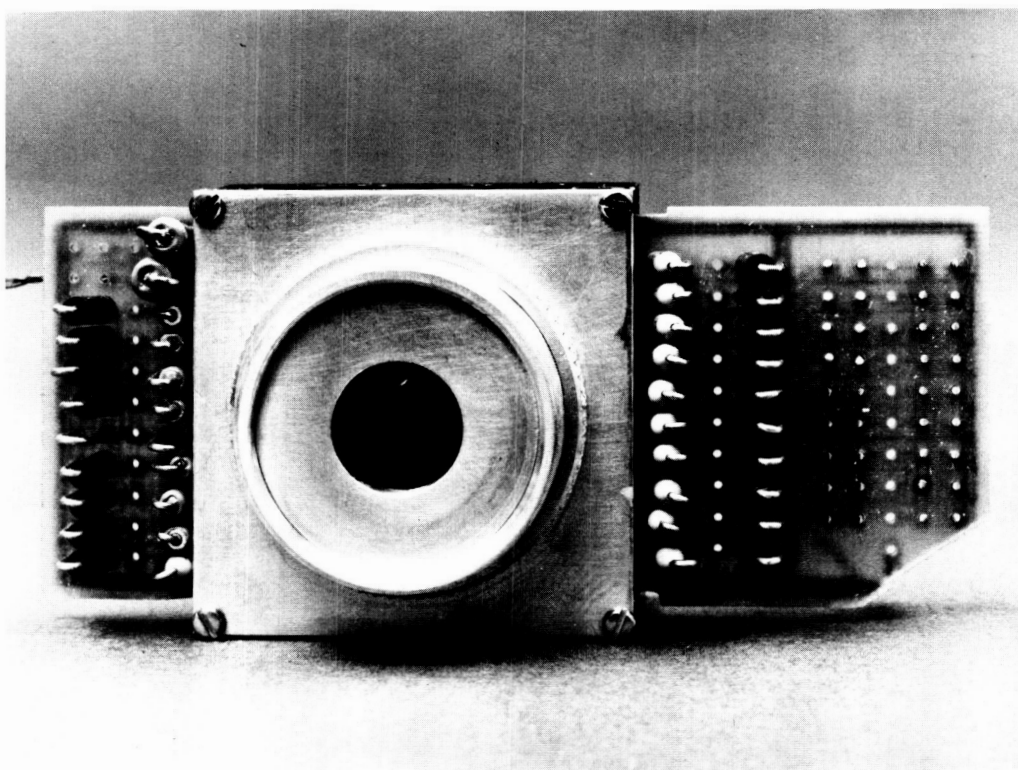


Figure 13. Array Cold Snout and Cover.

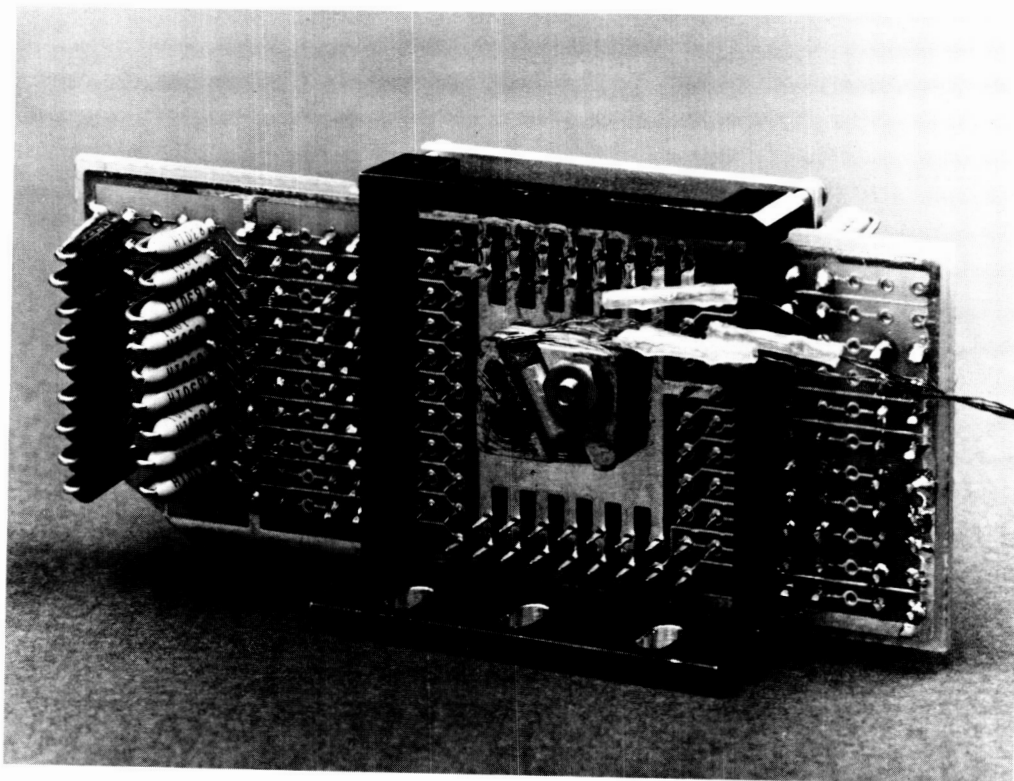


Figure 14. Focal Plane Mount (Back Detail).

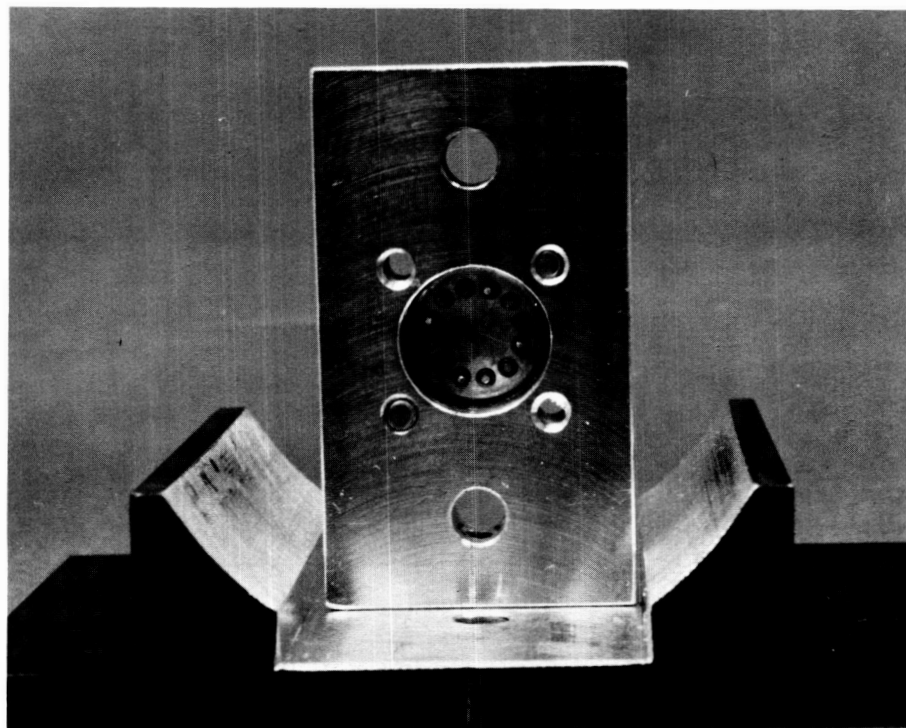


Figure 15. Internal Reference Source.

The thermal reference source suspended on wire leads is 1 mm square. It is mounted on the optic axis of the focal plane module. Not shown in the detail are the source cold filters and apertures used to set the flux level and spectral range.

INTERNAL REF SOURCE CALIB

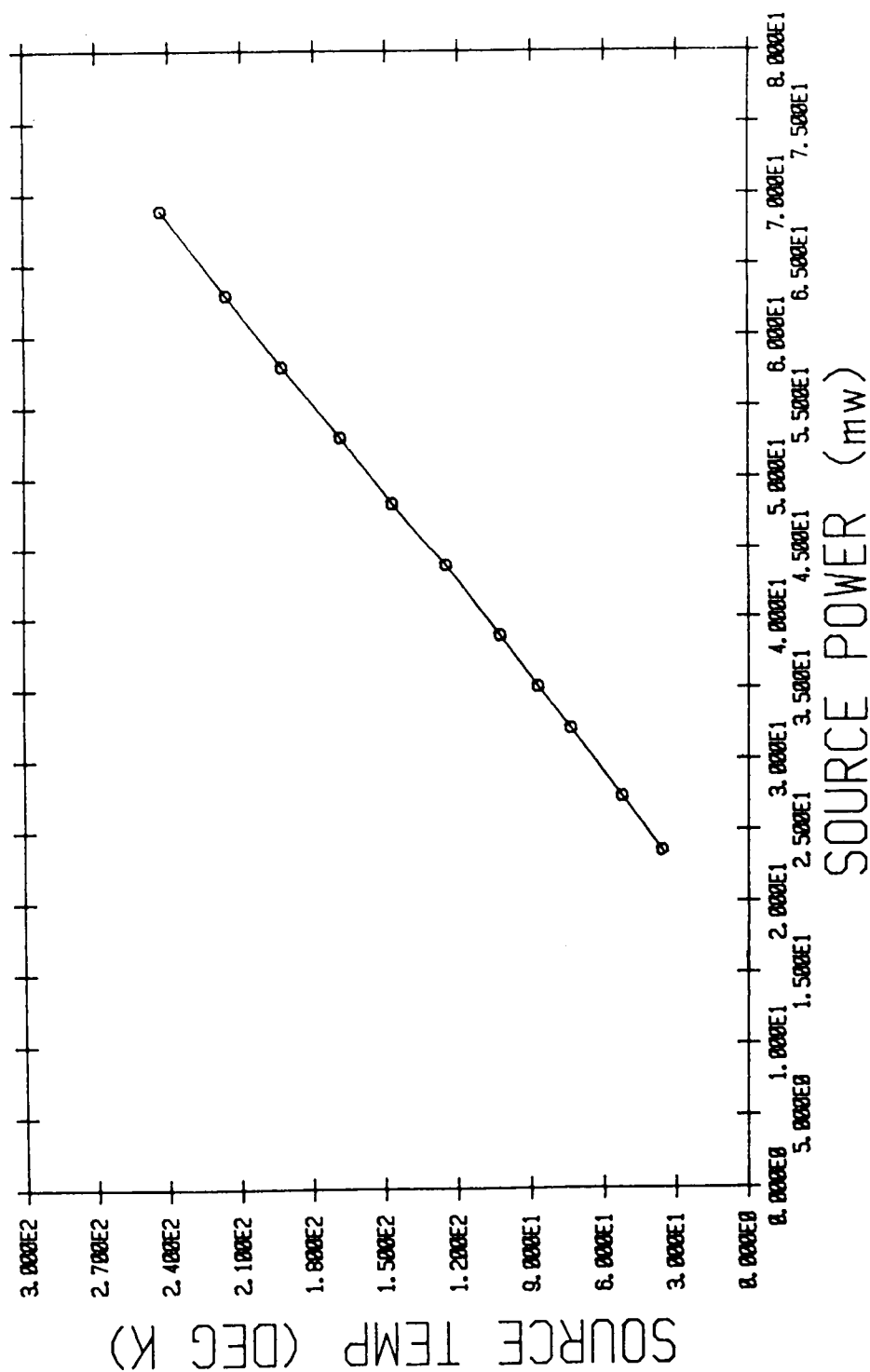


Figure 16. Internal Reference Source Calibration.

The internal reference sources (#IRS6) temperature verses the dissipated power for a bath temperature of 4.2 K and a 400 Ohm resistance. The temperature monitor is a silicon diode bonded to the source.

ELECTRONIC SYSTEM

A schematic of the complete system is shown in Figure 17. The array with multiplexer is inside of the dewar. Mounted at the side of the dewar are the clock timing interface circuits and the low noise warm preamplifiers. The data acquisition system (1-4) includes an analog processor, digital preprocessors, a timing generator, and a super minicomputer system.

Data was acquired by the following process. The timing generator was running continuously at a user selected integration time or frame rate. The array address was scanned sequentially from the beginning to end in a time multiplexed serial manner. The signals from the even and odd channels were amplified in the warm preamplifiers and then filtered in the analog signal processors. The resulting signal was digitized to 12 bits and then processed in the digital preprocessors. The operator using one of the application programs initiated the interactive data acquisition process. The resulting pictures were stored in the minicomputer hard disk memory. Pictures were taken then post processed using the data analysis programs.

Timing Generator

Timing was generated in a separate generator. Though the address codes could be generated in the minicomputer through a preprocessor, the noise and interference in our setup were noticeably worse. As a result the data reported here was taken using the separate timing generator.

The timing was based on the cyclic scanning of three nested 16 bit wide, electrically alterable read only memories, where each bit is assigned to a particular clock waveform. The memory scanned at the highest rate supplies the analog processor timing and unit cell functions. The next memory is the column address memory. The slowest is the row address memory. The timing can be referenced to an internal crystal oscillator running at 4 MHz for a time resolution of 500 ns or an external clock for variable time resolution. Many timing sequences can be stored in the generator memory by changing the start address with the mode select switch. The present system has a time multiplexed readout mode only. For this mode the N array columns are readout for each M row clocks. The integration time for an observation is determined from reset to reset of a particular pixel. An alternate readout involves integrating signals on the detectors for the duration of the integration time and rapidly reading out the stored results in a burst fashion. The time multiplexed readout mode of operation was chosen over a burst readout mode to eliminate the undesirable effect of burst readout on the focal plane temperature stability.

Using the internal clock, the available range of full array integration times is from less than .5 to slightly greater than 1800 seconds per frame set by thumbwheel switches on the timing generator. By selecting a subset of the full array with the mode select capability, the integration times can be reduced by the ratio of pixels addressed. For the majority of noise tests the corner 16 x 16 sub array was selected. The corresponding integration times available were from 0.04 to 134 seconds. The integration time used in an observation is determined by the size of the array, the incident flux rate and the array saturation level.

The dewar timing signals are optically isolated from the electronics at the timing buffer box, to minimize noise pickup. Also, the array bias and clock drive levels are connected at this point. Low noise power supplies have been used for these biases.

Warm Preamplifier

The warm preamplifiers for each channel are located at the dewar to minimize array loading and noise pickup. A schematic of the circuit used for each is shown in Figure 18. This amplifier interfaces the DRO array described above to the down-stream electronics.

An ultra stable, low noise, precision operational amplifier (PMI OP-27) was selected for the warm preamplifier. As described in the cryogenic preamplifier section the array output is a pulse amplitude modulated signal on a large DC offset. An AC coupled preamplifier was selected to provide the maximum gain while blocking the DC offset. The voltage gain (Gpa) is set by the feedback resistance and input resistance R_f & R_i respectively. The corresponding bandwidth is from less than 0.2 Hz to 220 KHz. The cut-on frequency is 0.2 Hz, set by the array output impedance, the protection resistances R_1 & R_2 , and the coupling capacitance C_i . The cutoff frequency is set by the feedback resistance R_f and the feedback capacitance C_f . The feedback capacitance can be changed at the warm preamplifier to adjust the noise bandwidth. The range is selectable from 220 KHz to 2 KHz in fixed increments.

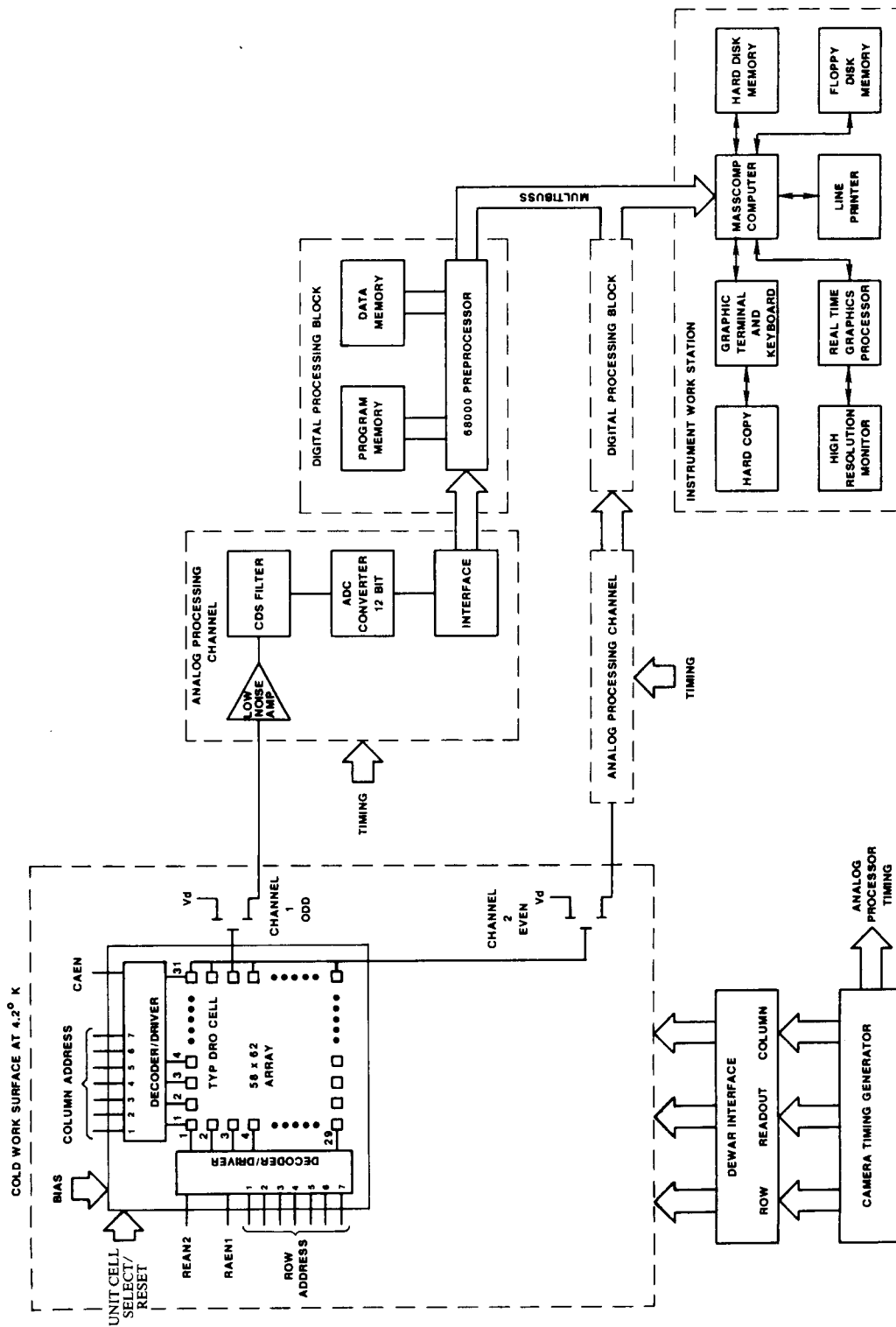


Figure 17. Electrical Block Diagram.

The array within the dewar is driven by a separate timing generator. The signals, an even and an odd channel, are fed into low noise warm preamplifiers. The preamplified signals are filtered by the analog processor and are digitized to 12 bits. The digital processor is a Motorola 68000 microcomputer. The processed digital information is fed into a Masscomp minicomputer system.

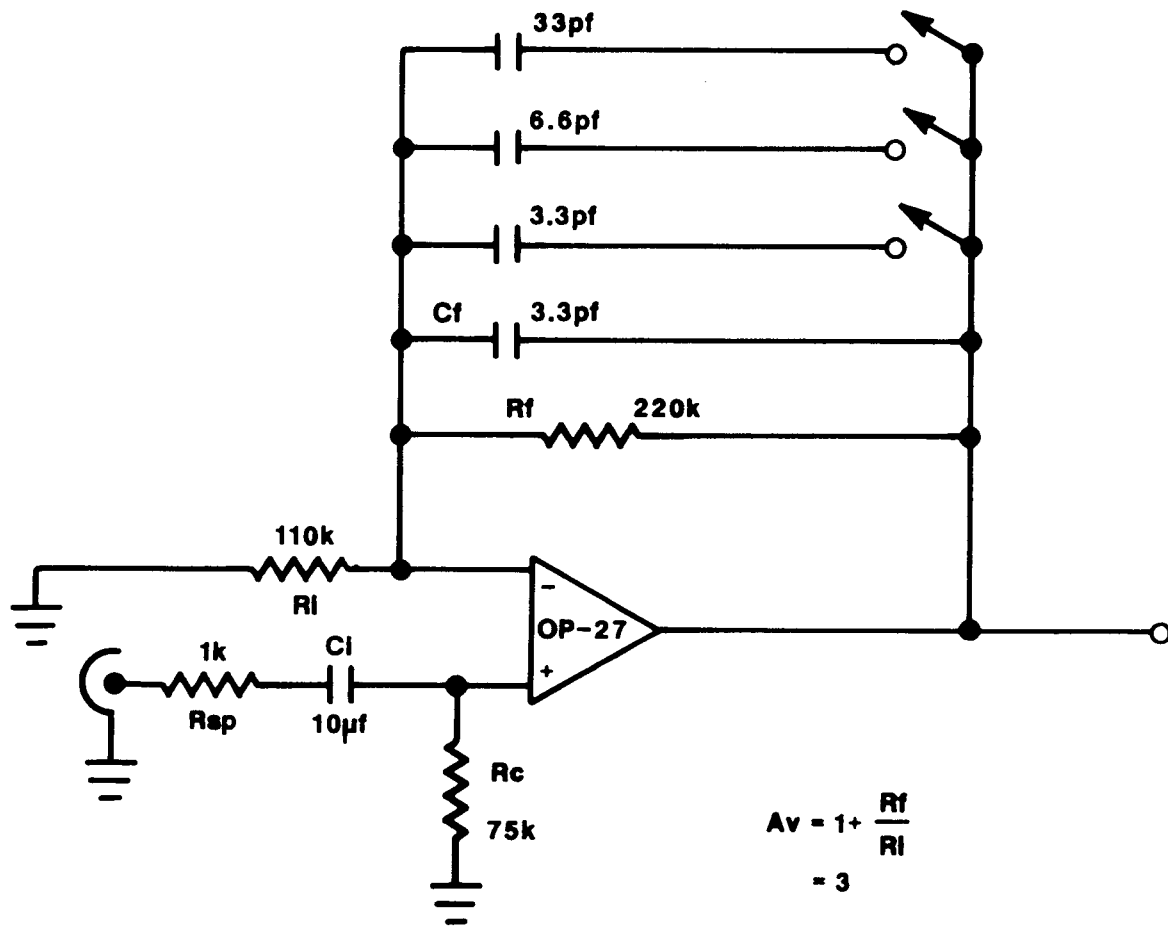


Figure 18. Preamplifier Schematic.

The noise equivalent circuit is shown in Figure 19 along with the expression for the net equivalent input noise. The estimate of the equivalent input warm preamplifier noise is:

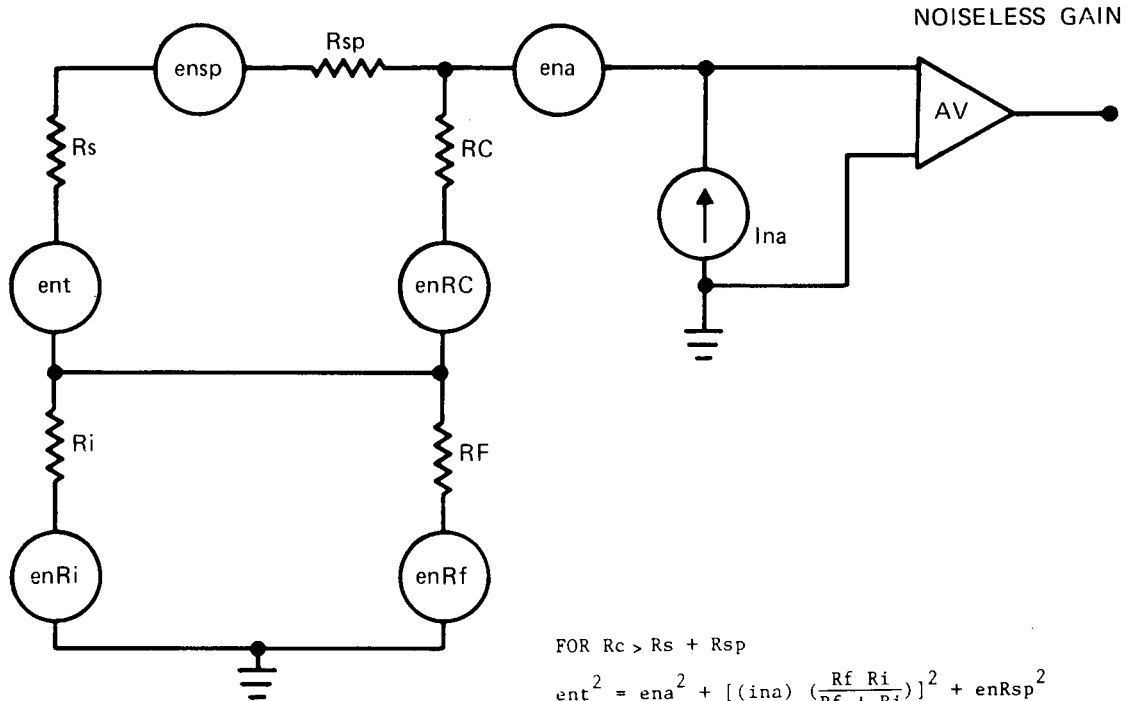
$$N_{pa} = 1/(Se G_{dro}) \left\{ \int_0^{\infty} [ent |T(s)|]^2 df \right\}^{1/2}$$

Where:

- ent = defined in Figure 19
- T(s) = analog processor transfer function
- BW = 220 kHz for preamp.
- Gdro = 0.7
- Se = 1.12 microvolt/electron

Analog Signal Processor

The signals from the array are time-amplitude-modulated by the address and readout clocks. A unique sampling filter (10) known as a correlated double sampling (CDS) filter is used to extract the signal, remove the reset noise component, and suppress any 1/f noise in the DRO cryogenic preamplifiers. A modification of the basic technique is used in the implementation of this filter with a DRO device.



$$\begin{aligned}
 &\text{FOR } R_c > R_s + R_{sp} \\
 &ent^2 = ena^2 + [(ina) \left(\frac{R_f R_i}{R_f + R_i} \right)]^2 + enR_{sp}^2 \\
 &+ [(enR_c) \left(\frac{R_s + R_{sp}}{R_s + R_{sp} + R_c} \right)]^2 + [(enR_i) \left(\frac{R_f}{R_i + R_f} \right)]^2 \\
 &+ [(enR_f) \left(\frac{R_i}{R_i + R_f} \right)]^2
 \end{aligned}$$

Figure 19. Preamplifier Equivalent Noise Circuit.

The operation of the filter is as follows (refer to Figure 20). The DRO circuit is simply a capacitor integrator which is reset after each integration. The pixel is read out and reset during the pixel readout time which is short compared to the integration time. To remove the reset noise component associated with the node capacitance, the reset level at the beginning of each integration must be subtracted from the signal value at the end of that integration. The two samples occur at the beginning and end of the integration time, which can extend to many seconds. To directly difference two samples over such long intervals requires extremely low $1/f$ noise in the DRO circuit. This is not the case for MOSFET devices. To minimize the FET $1/f$ noise, the sampling interval needs to be short so that differences suppress low frequency components. To accomplish both objectives, a comparison technique is applied where the signal is compared to a stable reference and the reset level is compared to a stable reference. The reference selected is the reset potential VRSTUC when reset (ORSTUC) is applied.

Signal Response

Refer to the simplified block diagram shown in Figure 20 and assume all gains are unity. The reset level reference for any pixel n is digitized at the start of the integration and stored in the digital processor memory. This reference is the difference between the baseline level and the offset level, where the baseline level (VBL) is the array output with the reset potential level applied (VRSTUC). During this interval S1 and S2 are closed, and Ch charges up to:

$$V_x(n) = V'BL(n) - VOS(n)$$

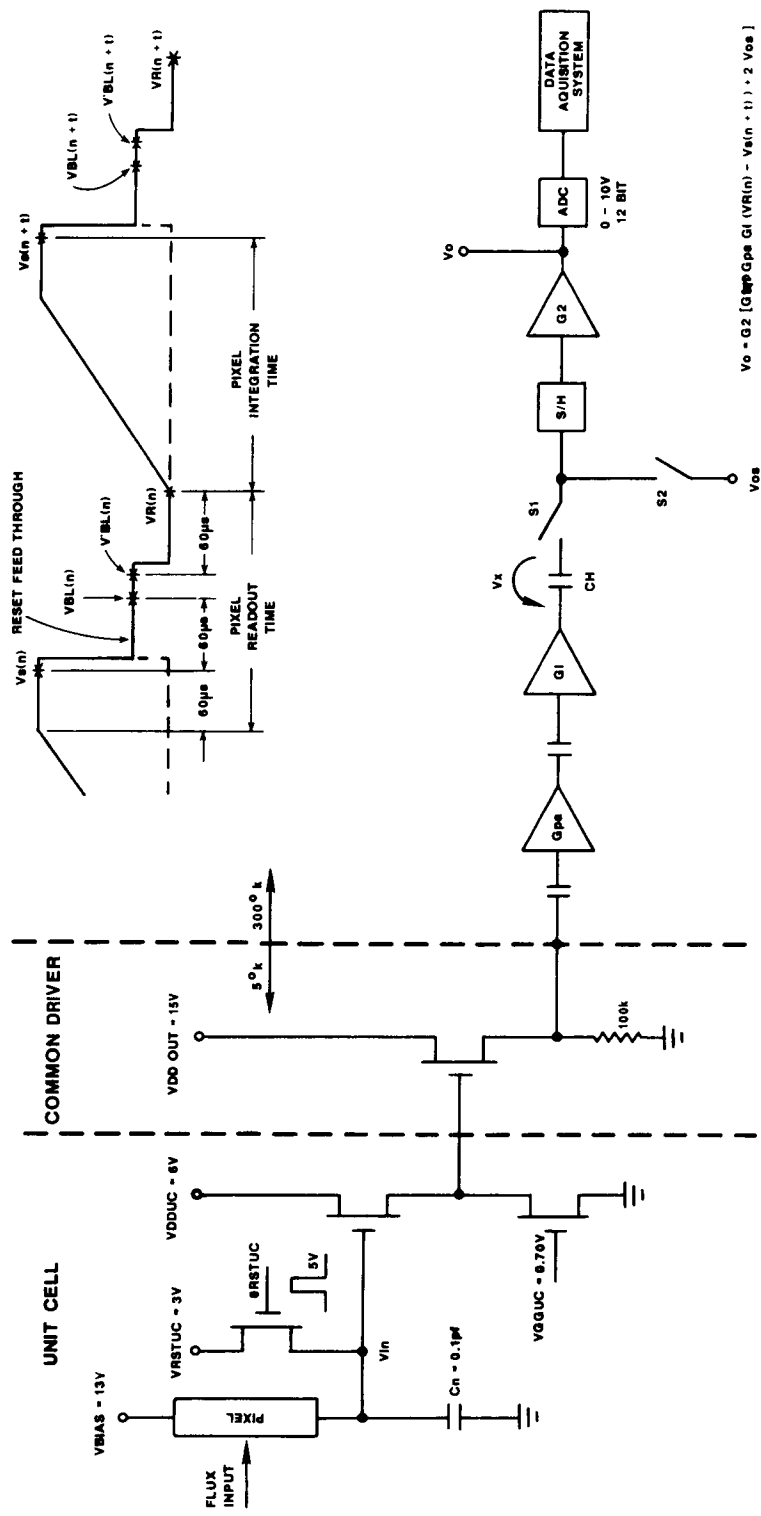


Figure 20. Simplified Block Diagram.

This operation stores the analog value of the baseline level minus the offset level on capacitor Ch. The reset pulse is removed and the reset level is sampled with S1 closed and S2 open. The output voltage is the reset level minus the stored value:

$$V_o(n) = V_R(n) - V'_{BL}(n) + V_{OS}(n)$$

At the end of the integration sample of the signal is taken with respect to the baseline level. Again S1 and S2 are closed and Ch charges up to:

$$V_x(n+t) = V_S(n+t) - V_{OS}(n+t)$$

The signal level minus the offset level is stored on capacitor Ch. The reset pulse is applied and the baseline level is sampled with S1 closed and S2 open. The output voltage is the baseline level minus the stored value:

$$V_o(n+t) = V_{BL}(n+t) - V_S(n+t) + V_{OS}(n+t)$$

The signal at the start of the integration ($V_o(n)$) and the signal at the end of the integration ($V_x(n+t)$) are digitized, stored and summed in the digital preprocessor. Assuming that the offset levels and baseline levels do not vary with time, the sum of the output signals in the digital processor is:

$$V = V_R(n) - V_S(n+t) + 2 V_{OS}$$

Where:

$$V_{BL}(n) = V_{BL}(n+t) \text{ and } V_{OS}(n) = V_{OS}(n+t)$$

Including the effects of the gain stages the signal transfer function becomes:

$$V = G_2 \{G_t [V_R(n) - V_S(n+t)] + 2 V_{OS}\}$$

Where:

$$G_t = G_{dro} G_{pa} G_l$$

For this analog processor the digital full scale (bin 4096) is set at zero signal level and digital zero (bin 0) is at full signal level.

Noise Response

For each sample uncorrelated noise is transferred through the system with a characteristic transfer function (10) as follows:

$$T(s) = T_o[1 - \text{EXP}(-sT_{cds})]/(1 + s/2\pi BW)$$

Where:

- T_o = signal gain
- T_{cds} = time from end of clamp to end of sample
- = 60 microseconds
- BW = preamplifier bandwidth
- = 220 KHz

For a gain of 1, a plot of the square of the magnitude of the transfer function is shown in Figure 21. The principal

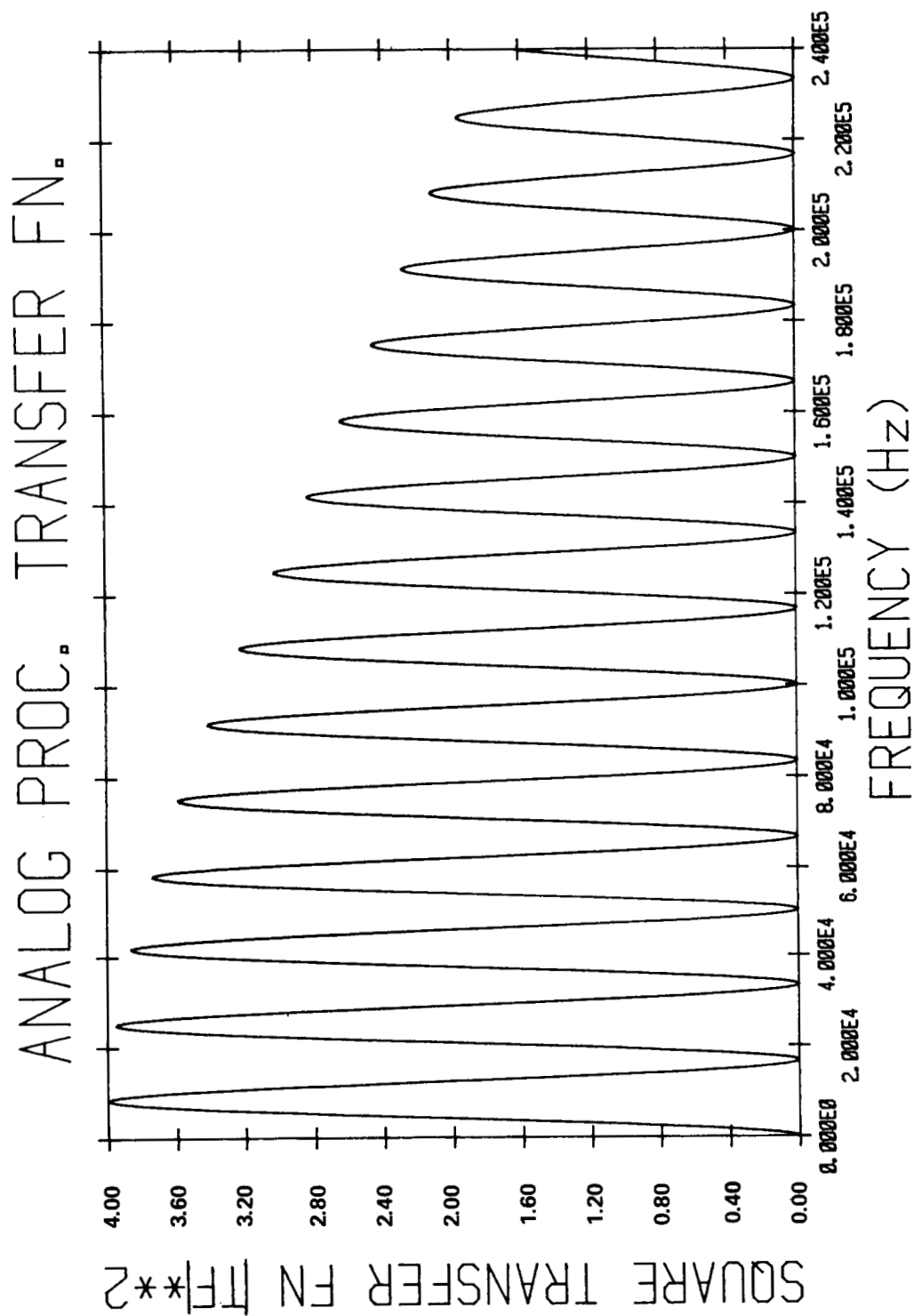


Figure 21. CDS Transfer Function.

features of this filter are the zeros at zero frequency and harmonics of the sampling frequency and the primary transmission lobe. The effect of the CDS filter on $1/f$ noise in the cryogenic preamplifier or in the system is to suppress the low frequency components and to alias any components above the first null into the output. In effect very low frequency noise is not passed through the filter and it is this property that is used to suppress the low frequency $1/f$ component. Noise whose period is n times T_{cds} is also suppressed in the same way. To summarize, this sampled filter technique effectively restores the video reference, removes the detector reset noise, and suppresses the DRO NMOS transistor $1/f$ noise.

The ideal quantization error due to the digitization process in the analog processor is:

$$\begin{aligned} N_q &= FS / (12^{1/2} * 2^n * S_e * G_{dro} * G_{pa} * G_{cds}) \\ &= 75 \text{ e rms per digital conversion} \end{aligned}$$

Where:

$$\begin{aligned} FS &= \text{ADC full scale voltage range} \\ n &= \text{ADC \# bits} \\ G_{pa} &= \text{warm preamplifier gain} \\ &= 3 \\ G_{cds} &= \text{analog processor gain} \\ &= 4 \end{aligned}$$

DIGITAL SYSTEM

The digital system includes a first-in, first-out buffer memory (FIFO), digital preprocessors, and a multibus-based minicomputer system.

The FIFO memory buffers and synchronizes the time-multiplexed array data from the latched ADC to the digital preprocessors. The preprocessors are Motorola 68000 microcomputers interfaced to the multibus backplane in the minicomputer system. The user interface to the system is through the Masscomp minicomputer. This includes a hard disk memory for data storage, a floppy disk, Tektronix color graphics terminal, and Tektronix color printer.

SOFTWARE

The system is set up to operate under UNIX and the application programs are programmed in the 'C' language. Two programs, NOISE and IMAGE, were used to acquire and analyze data.

The NOISE program was set up to take temporal data at the selected frame rate from a single pixel and create data files with up to 1024 samples. These samples were then displayed in time or Fast Fourier Transformed and displayed to study the noise in the array.

The IMAGE program was set up to take spatial data from a 16 x 16 subset of the array. Files of pictures were acquired, accumulated and analyzed using this program.

EXPERIMENTAL PROCEDURE

The array was cooled over night before testing to allow the thermal background level to drop to a level where it did not effect dark current measurements. Careful attention was paid to grounding to prevent both ground loops and pickup interference.

The thermal response of the array is shown in Figure 22. The overshoot in the thermal response of the focal plane on application of the array power is not understood at this time. The response of the array to a step increase in power dissipation in the heater is shown in Figure 23 and represents a simple single time constant system response. The effects of thermal response of the focal plane array to changes in the detector bias, integration time, and internal reference source was minimized when the data was taken after a 3 minute delay.

The parameters that were varied for the read noise and dark current tests were the focal plane temperature and the integration time. The detector bias was set either to 0 volts or 10 volts across the detector. From earlier tests this bias

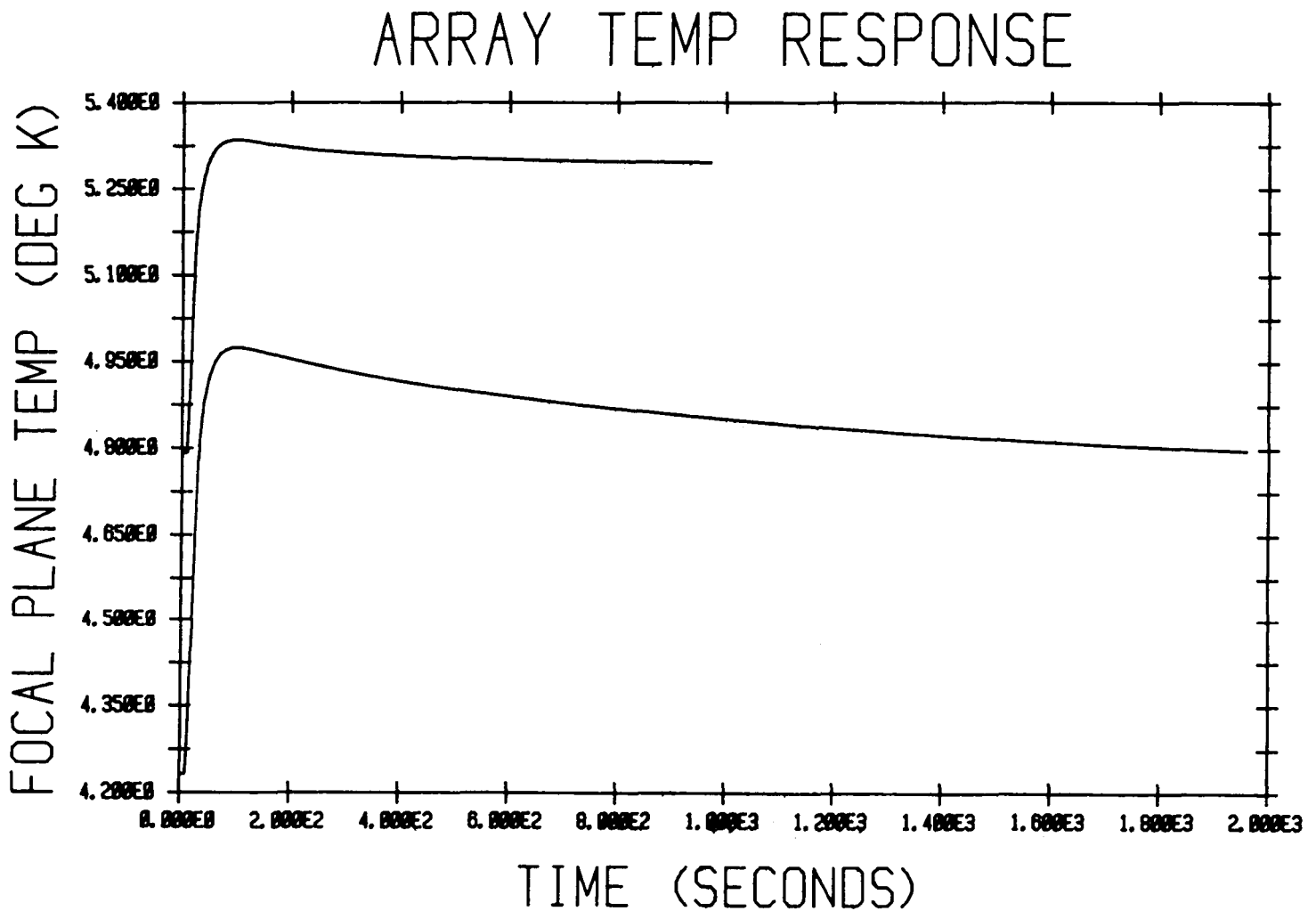


Figure 22. Focal Plane Temperature Response. The thermal response of the focal plane module to the application of power is indicated in these two traces. Starting from a bath temperature of 4.2 K, the lower trace highlights the thermal response to the DC power for the unit cells and output drivers (no clocks). The overshoot is clearly evident. A long response tail is also seen extending out to 2000 sec. The upper trace is the response with the application of the clocks for a frame rate of 26 f/s.

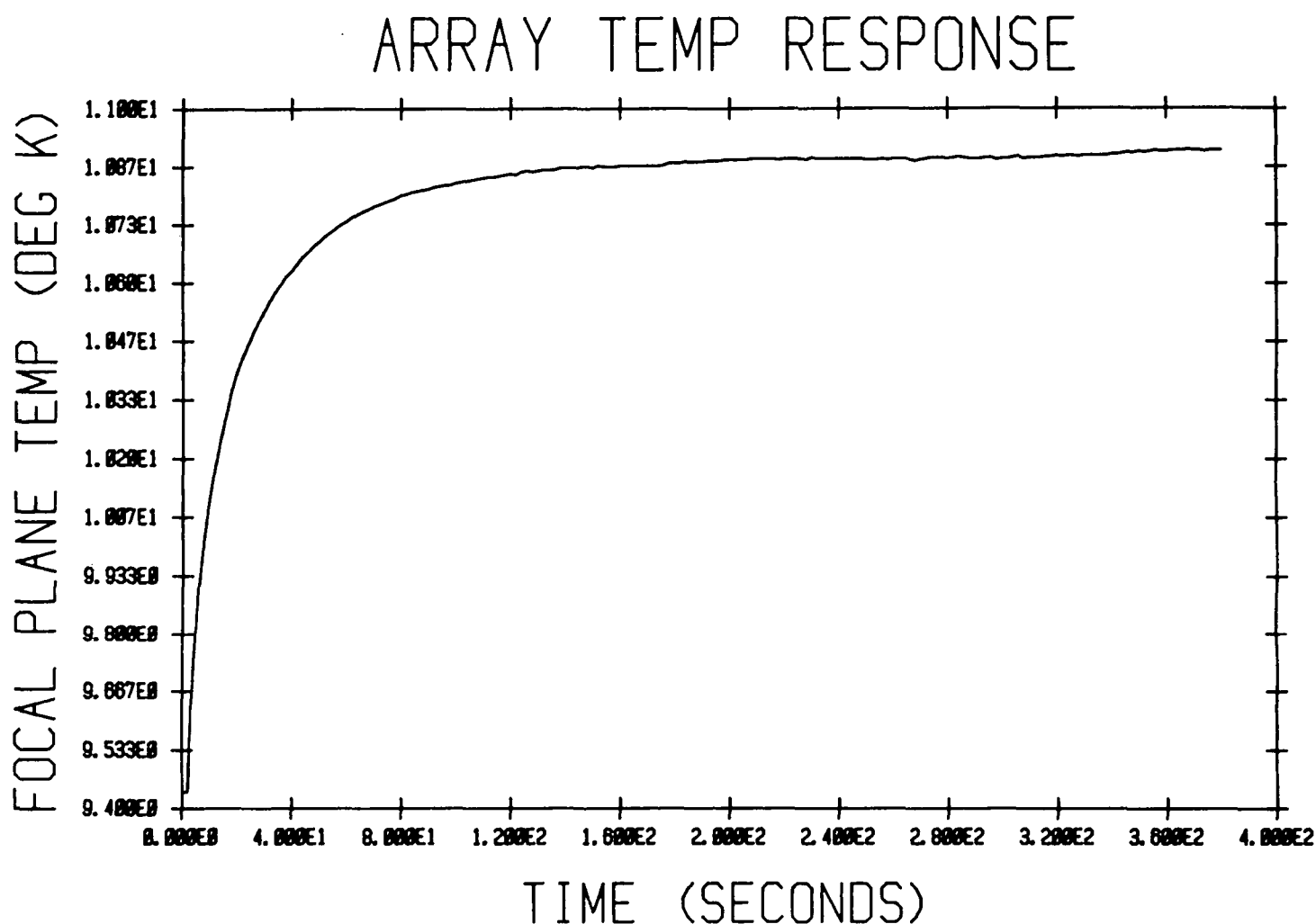


Figure 23. Focal Plane Heater Response.

The thermal response to a 25 mW step input in the heater resistor.

was determined to give the best response for these backgrounds and temperatures. Tests for response to the internal thermal reference source were conducted to ensure that the array was not operating in saturation.

Data from both a reference pixel and a subset of the 58 x 62 array were taken. Inoperative pixels and pixels with excessive read noise or dark current were avoided in selecting the reference pixel. A subset of the array was used for the imaging tests. The corner 16 x 16 subset including [1, 1] was used for these detailed tests. We found no indication of any extraordinary inoperative regions in the remainder of the array and it is felt that this subset is representative of the total array.

READ NOISE SUMMARY

Based on the above discussions, the equivalent input read noise referred to the sense node capacitance (C_n) can be predicted from a knowledge of the noise sources and the system transfer function. The noise sources affecting the read noise level are the sense node reset (kTC), the cryogenic DRO MOSFET preamplifier noise, and the system noise composed of the warm preamplifier noise, broadband noise in the analog processor, quantization error, DRO bias supply noise, and DRO clock noise.

The sense node kTC reset noise determined above is 18 e rms. The digital algorithm and sampling technique used are designed to remove the reset noise since it is correlated within a sample.

The DRO NMOS transistor noise is primarily $1/f$ throughout the system signal bandwidth. The effective rms noise per digital conversion due to the DRO NMOS cryogenic preamplifier is the integral of the product of the noise spectrum and the CDS transfer function (Figure 24). For the noise spectrum of the DRO array amplifier (including the four MOSFET transistors discussed above) this is calculated to be 34.6 e rms for each digital conversion. Since the DRO signal is sampled at the beginning and at the end of the integration for the digital processing algorithm used, the total noise introduced through processing is root 2 times larger or 49 e rms.

Noise in the warm preamplifier is also processed through the analog processor in an identical manner as the DRO NMOS transistor noise. The equivalent input noise for the filtered warm preamplifier noise is 34.4 e rms per digital conversion and 48.6 e rms using the digital algorithm.

For the low input preamplifier gain ($G_{pa} \times 3$) the filtered broadband noise contribution from the analog signal processor can not be ignored and the equivalent input charge is 59.4 e rms per digital conversion and 84 e rms using the digital algorithm.

Also, due to the low front end gain and the 12 bit range in the data acquisition system, the quantization error contributes 75 e rms per digital conversion and 106 e rms using the digital algorithm. The contributions to read noise from the DRO bias supplies and the clocking noise have not been completely investigated. However, in the summary the limits to excess noise sources are defined.

The system noise sources are summarized in Table 4. The total expected system noise is the quadrature sum of the warm preamplifier noise, the analog processor broadband noise, and the quantization error, and is 144 e rms. The system noise was measured before turning on the array. This was done with the array attached to the warm preamplifier but no bias or clocks on the array. The measured system noise contribution, listed in Table 4, is 127 e rms at best and 164 e rms at worst. In excellent agreement with expectations.

Table 4. System Noise Summary for Preamplifier Gain $\times 3$

Component	Per ADC Conversion	With kTC Removed
N _{pa}	34.4	48.6
N _{cds}	59.4	84
N _{qi}	75	106
Total		143.7 calculated
Measured System Noise		127 best 164 worst

A 16 bit ADC analog processor is currently under development to reduce the quantization error term, and by band limiting the input of the analog processor that noise term can be reduced. But using the current warm preamplifier gain, the expected system noise will be 15 e rms by reducing the values of R_i and R_f and minimizing their thermal noise contribution.

Though the current system noise is in excess of what can be achieved, the noise roughly doubled in turning on the array. This allowed a determination of the array's read noise performance for these tests. In reporting array read noise results, the system noise was removed in quadrature from the measured results to determine the array contribution.

The DRO DC biases were applied and the noise was again measured after the temperature stabilized. This gave an indication of the read noise with the DRO multiplexer disabled but the DRO driver was on. The clocks were then applied and the noise was again measured after the temperature stabilized. This was done with the net detector bias set to zero or the integration time minimized to eliminate the detector dark current from the read noise measurement. This

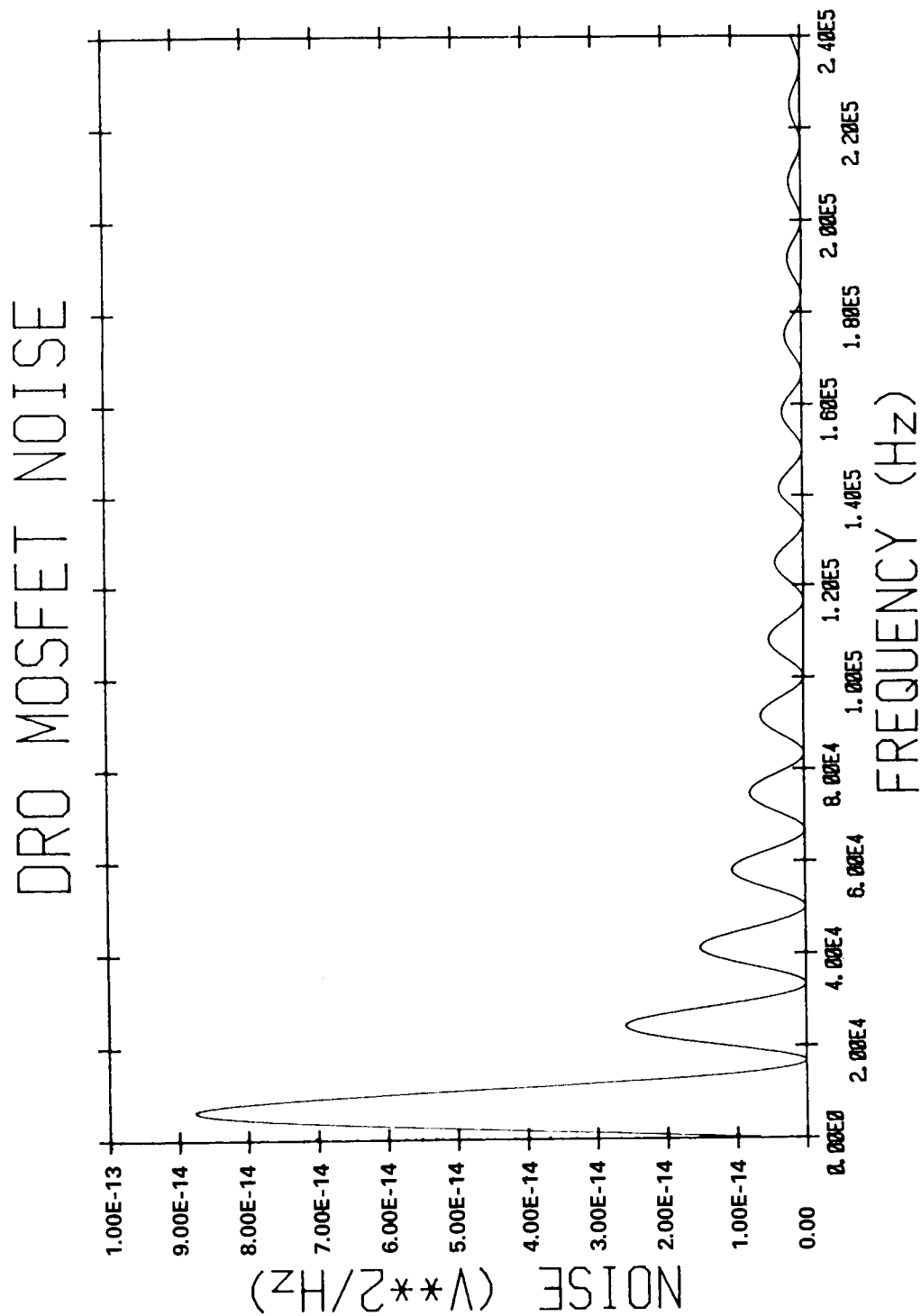


Figure 24. CDS MOSFET Noise Response.

Product of the DRO MOSFET transistor noise and the analog processor transfer function.

noise data was taken looking at the reference pixel [4, 4] where a temporal record of up to 1024 samples were taken. The measured noise performance at a focal plane temperature of 5.4 K and with the net detector bias set to zero is summarized in Table 5.

Table 5. Read Noise Summary at 5.4 K.

Component	Per ADC Conversion	With kTC Removed
NkTC	18	0
Nfet	34.6	49
Nbias	TBD	TBD
Nclock	TBD	TBD
Total (DRO MOSFET limited)		49 calculated
Measured DRO with bias only*		123 best 214 worst
Measured DRO full up*		256 best 424 worst

* System noise was removed in quadrature from reading. (127 crms best, 164 crms worst)

* Read noise decreased by 30% @ 12°K. See Figure 25.

To study the low-background, low-temperature noise, three noise tests were conducted: read noise versus focal plane temperature, read noise versus integration time, and noise versus background photo flux.

The read noise of the reference pixel [4, 4] was measured as a function of the focal plane temperature (Figure 25). The integration time, minimized to prevent the array dark current from contributing to the results, was 34.7 milliseconds. The residual photon flux was any background present in the dewar and was minimized to make a negligible contribution to the result. The results are plotted both with and without net detector bias applied. The improvement with net detector bias is frequently noted but not understood. In both cases the read noise showed an improvement as the temperature increased to about 15 K then degraded above 15 K. For the bias applied case the improvement was from 30-40% to 170 e rms in going from 5.4 kelvin to 8-12 kelvin.

The read noise of reference pixel [4, 4] was measured versus the integration time at an operating temperature of 5.4 K. Figure 26 is the noise plot for an integration time of 34.7 milliseconds. Figure 27 is the noise plot for an integration time of 1 second. As the integration time was increased the drift dominated the standard deviation as seen in Figure 27. However, the white noise component remained essentially the same. Noise measurements beyond 1 second were dominated by excess low frequency drift. This drift has been traced to temperature dependent gain variations in the analog signal processor and are not attributed to the detector array.

The read noise of the reference pixel [4, 4] was measured versus the photon flux background from the unfiltered internal reference source (Figure 28). The increase in noise with background flux is evident with the noise doubling for a source temperature in the range of from 20 to 30 K. Since the source intensity is a very sensitive function of the source temperature on the exponential side of the Wien curve, an accurate determination of the source intensity was not possible.

An apertured and attenuated source operated on the power side of the Wien curve has been built to test the background limited noise performance of the DRO array. Results using the source in this mode will be reported in the future.

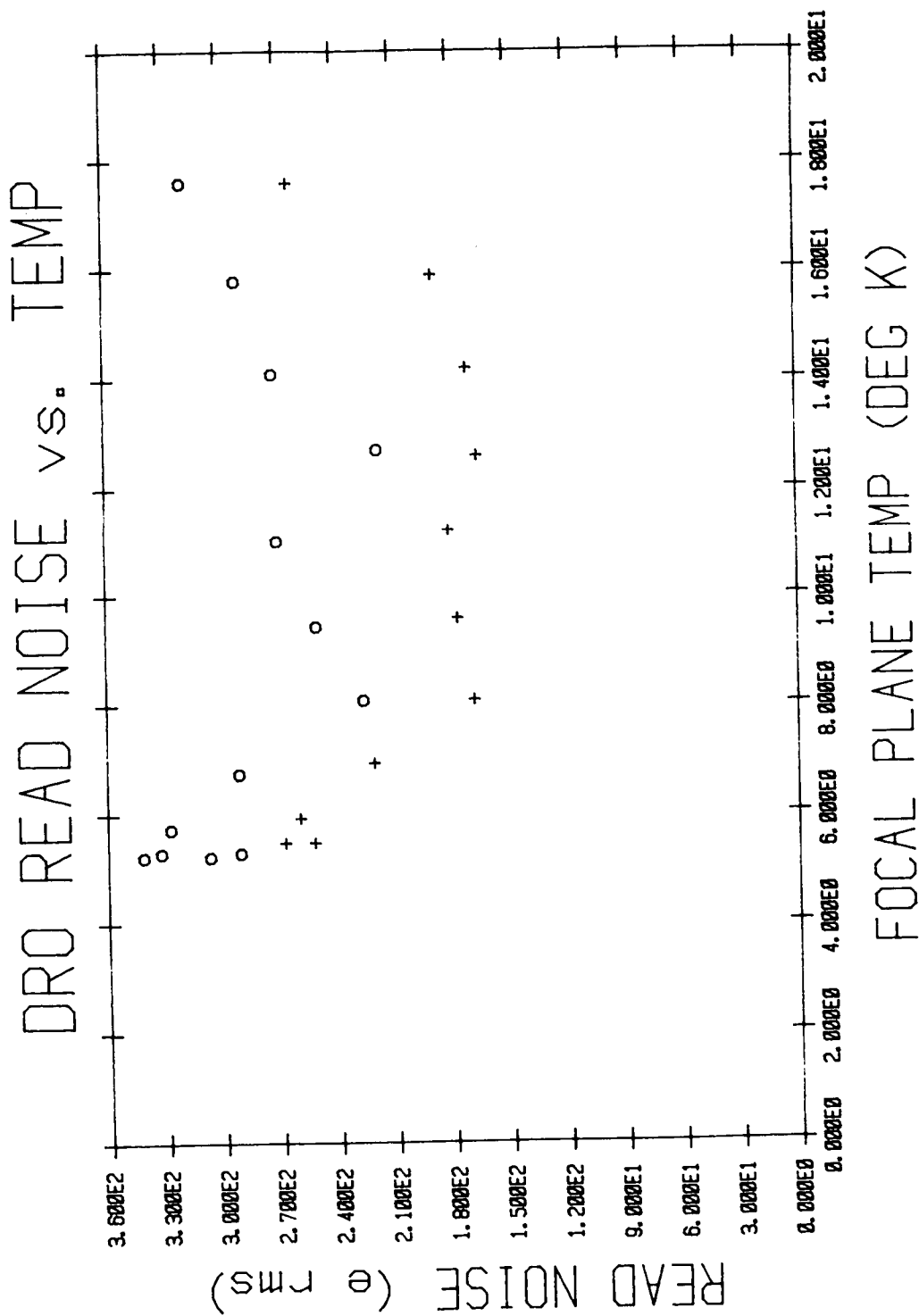


Figure 25. DRO Read Noise vs. Temperature.

Pixel [4, 4]
 Integration Time 34.7 milliseconds
 + Net Detector Bias E = 10 volts
 o Net Detector Bias E = 0 volts
 System Noise 139 e rms

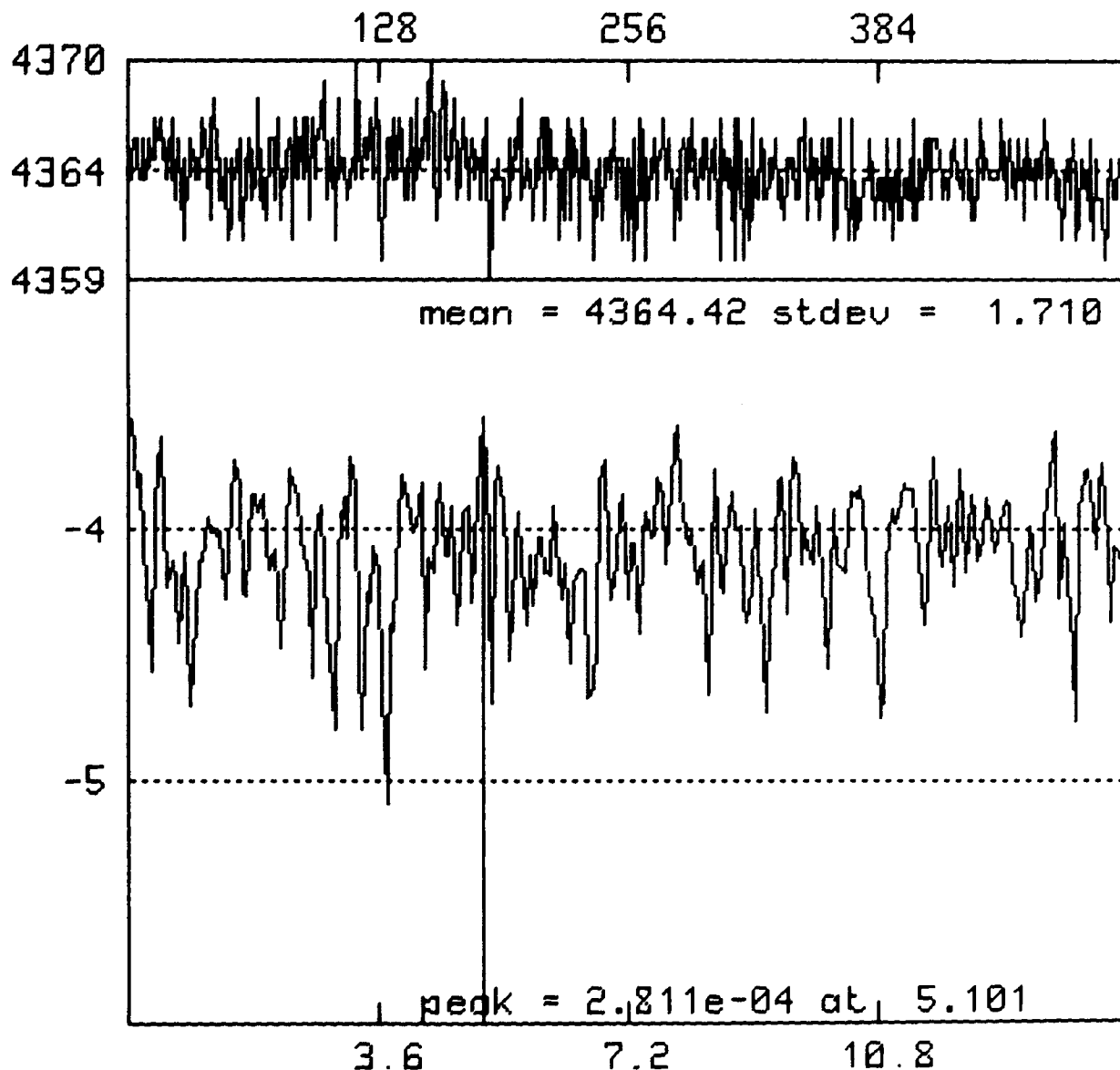


Figure 26. Read Noise Spectral Density Plot #1.

Pixel [4, 4]

Time trace: x = sample # y = bins

Standard Deviation noise in bins Nr = 311 e rms

ADC Bin sensitivity Sb = 182 e/bin

Spectral trace: x = frequency in Hz

y = input referred noise in volts/ $\sqrt{\text{Hz}}$

Focal Plane Temperature 5.4 K

Net Detector Bias E = 0 volts

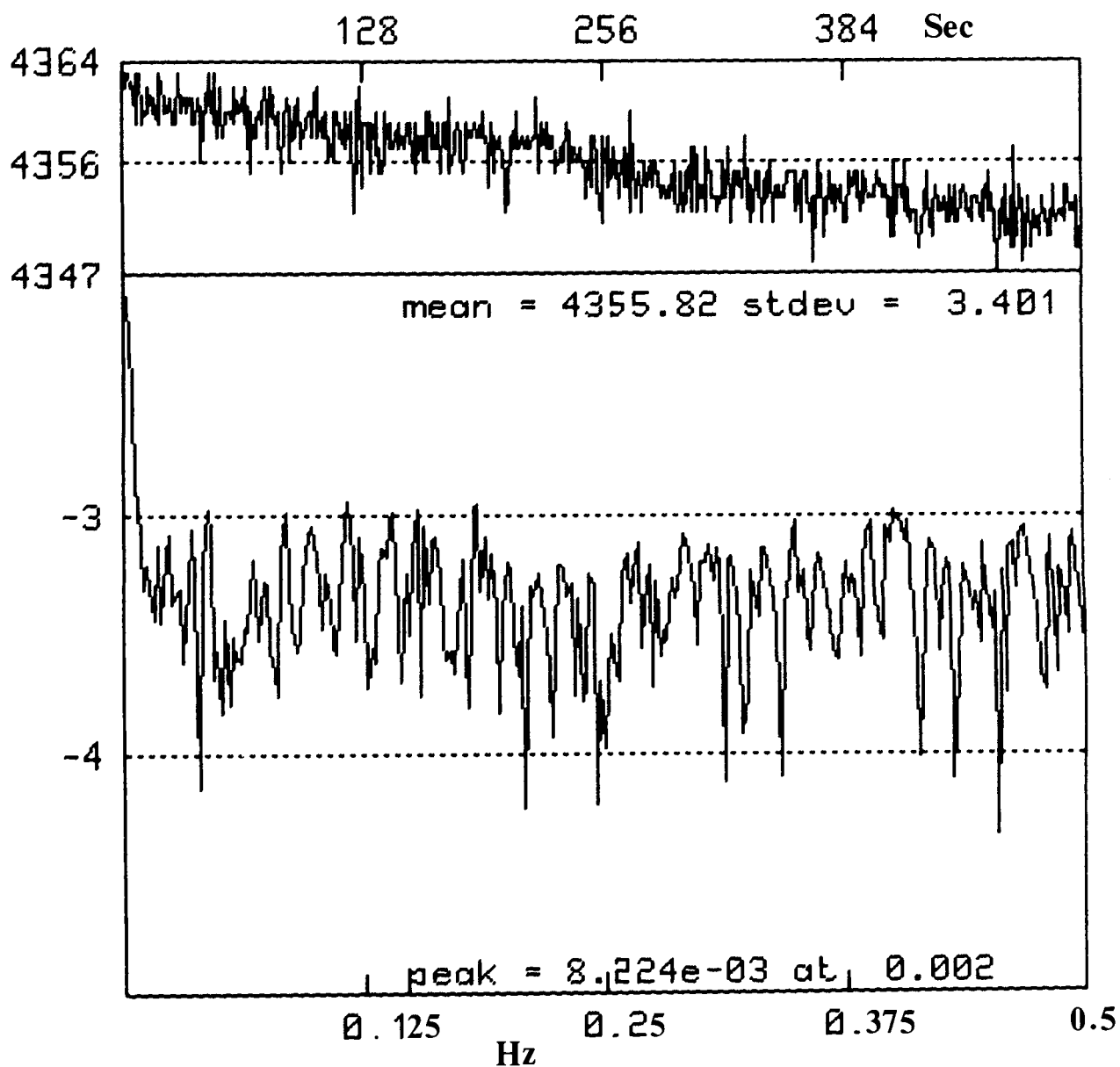


Figure 27. Read Noise Spectral Density Plot #2.

Pixel [4, 4]

Time trace: x = sample # y = bins

Standard Deviation drift dominated

ADC Bin sensitivity $S_b = 182 \text{ e/bin}$

Spectral trace: x = frequency in Hz

y = input referred noise in $\text{volts}/\sqrt{\text{Hz}}$

Focal Plane Temperature 5.4 K

Net Detector Bias $E = 0 \text{ volts}$

Graph showing Noise (e_{rms}) versus Power on Source (mw) for Source Temperature (K) values: 38, 47, 55, 64. The Y-axis ranges from 0.000E0 to 1.200E3. The X-axis ranges from 0.000E0 to 3.200E1. The data points show that noise increases with power, and higher source temperatures result in higher noise levels.

Power on Source (mw)	Noise (e_{rms}) at 38 K	Noise (e_{rms}) at 47 K	Noise (e_{rms}) at 55 K	Noise (e_{rms}) at 64 K
0.000E0	0.000E0	0.000E0	0.000E0	0.000E0
0.400E0	0.000E0	0.000E0	0.000E0	0.000E0
0.800E0	0.000E0	0.000E0	0.000E0	0.000E0
1.200E0	0.000E0	0.000E0	0.000E0	0.000E0
1.600E0	0.000E0	0.000E0	0.000E0	0.000E0
2.000E0	0.000E0	0.000E0	0.000E0	0.000E0
2.400E0	0.000E0	0.000E0	0.000E0	0.000E0
2.800E0	0.000E0	0.000E0	0.000E0	0.000E0
3.200E0	0.000E0	0.000E0	0.000E0	0.000E0
0.000E1	0.000E0	0.000E0	0.000E0	0.000E0
0.400E1	0.000E0	0.000E0	0.000E0	0.000E0
0.800E1	0.000E0	0.000E0	0.000E0	0.000E0
1.200E1	0.000E0	0.000E0	0.000E0	0.000E0
1.600E1	0.000E0	0.000E0	0.000E0	0.000E0
2.000E1	0.000E0	0.000E0	0.000E0	0.000E0
2.400E1	0.000E0	0.000E0	0.000E0	0.000E0
2.800E1	0.000E0	0.000E0	0.000E0	0.000E0
3.200E1	0.000E0	0.000E0	0.000E0	0.000E0

Figure 28. Noise vs. Background Flux.

Pixel [4, 4]	
Bin sensitivity	Sb = 182 e/bin
Integration Time	t = 34.7 ms
Focal Plane Temperature	5.4 K
Net Detector Bias	E = 10 volts
System Noise	Ns = 146 e rms

DARK CURRENT

Dark current measurements were taken by collecting 16 x 16 subarray images under different operating conditions for integration times up to 134 seconds. In taking images with this system we have noticed that the offset level is dependent both on integration time and array temperature.

The offset level is the output signal from the analog processor with the net detector bias set to zero. The typical offset response as a function of integration time is plotted in Figure 29. The offset response versus the focal plane temperature is plotted in Figure 30. To remove these offset components, data was taken as follows. First, an offset image (OS) was taken with the net detector bias set to zero. Next, a dark current image (DC) was taken with the net detector bias applied. Finally, a photo response image (PR) was taken with the net detector bias and the internal source on. In all cases data taking was delayed for a minimum of 300 seconds to allow the array to stabilize before images were taken. The difference between the dark current image and the offset image is the corrected dark current. The difference between the photo response image and the dark current image is the corrected photo response image.

For the reference pixel [4, 4], the DRO response versus integration time for both dark current and photon flux is shown in Figure 31. The dark response is very linear with time and for the reference pixel [4, 4] is 187 e/s per pixel. The photo response is less linear and output saturates at about 7×10^5 e limited by the analog processor dynamic range.

At this point, the flat field gain matrices are not accurate enough to correct for the array spatial gain variations. This has prevented a determination of the noise from spatial images. However, allowing for gain variations in the standard deviation, comparisons of the spatial average of the pixels in an image is possible. The plot in Figure 32 is a histogram of the spatial average of the DRO array dark current for an integration time of 134 seconds. The mean value and standard deviation for the distribution of dark currents are 318 e/s \pm 177 e/s respectively. The value for the reference pixel [4, 4] is within 1 sigma of the mean as indicated in the figure.

The spatial average of the dark count versus the integration time for the subarray is seen in Figure 33. Excellent linearity in integration time is seen with an average dark current of 337 e/s. The dark current of three pixels versus focal plane temperature, is plotted in Figure 34. The array response versus temperature was measured in separate tests to determine the effect on dark current of the detector photoconductive gain. The change in response with temperature was roughly 20% per degree with the response doubling in going from 6 to 16 K. This effect was not removed from this dark current data. The observed increase in current, however, is in excess of any photoconductive change and is attributed to the thermal generation of carriers at the operating temperature. The wide variation in dark current is indicative of localized sources of excess dark current.

An activation energy analysis of the dark current of pixel [8, 2] was conducted to try to identify the source of dark current. A plot of the dark current versus 1/temperature is shown in Figure 35. The slopes for gallium, and boron impurities are included for comparison. The slope of the dark current for the 10.24 second integration time at a temperature of 15 K indicates that the dark current is not due principally to gallium but a shallower impurity (possibly boron) present in the detector. There is some offset in the data for integration times of 10.24 and 134 seconds. A constant dark current with 1/temperature is indicative of a light leak or resistive shunt. The existence of some residual light leakage in the 134 second low temperature dark current is evident in Figure 35. Therefore, the quoted dark currents in this report can only be considered worst case results.

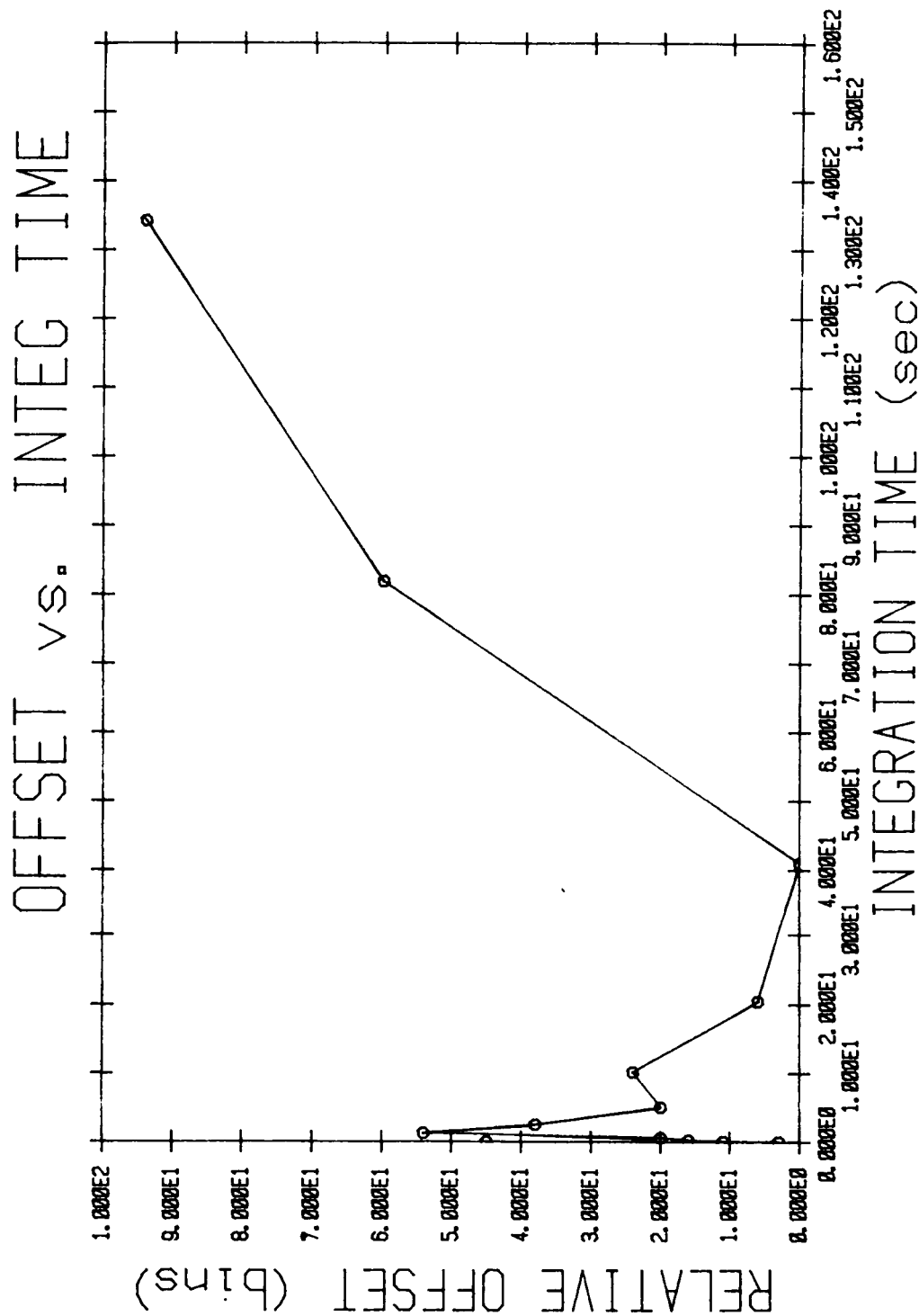


Figure 29. Relative Offset Level vs. Integration Time.

Pixel [4, 4]
 Bin sensitivity Sb = 182 e/bin
 Focal Plane Temperature 5.4 K
 Net Detector Bias E = 0 volts
 Error ± 1 bin

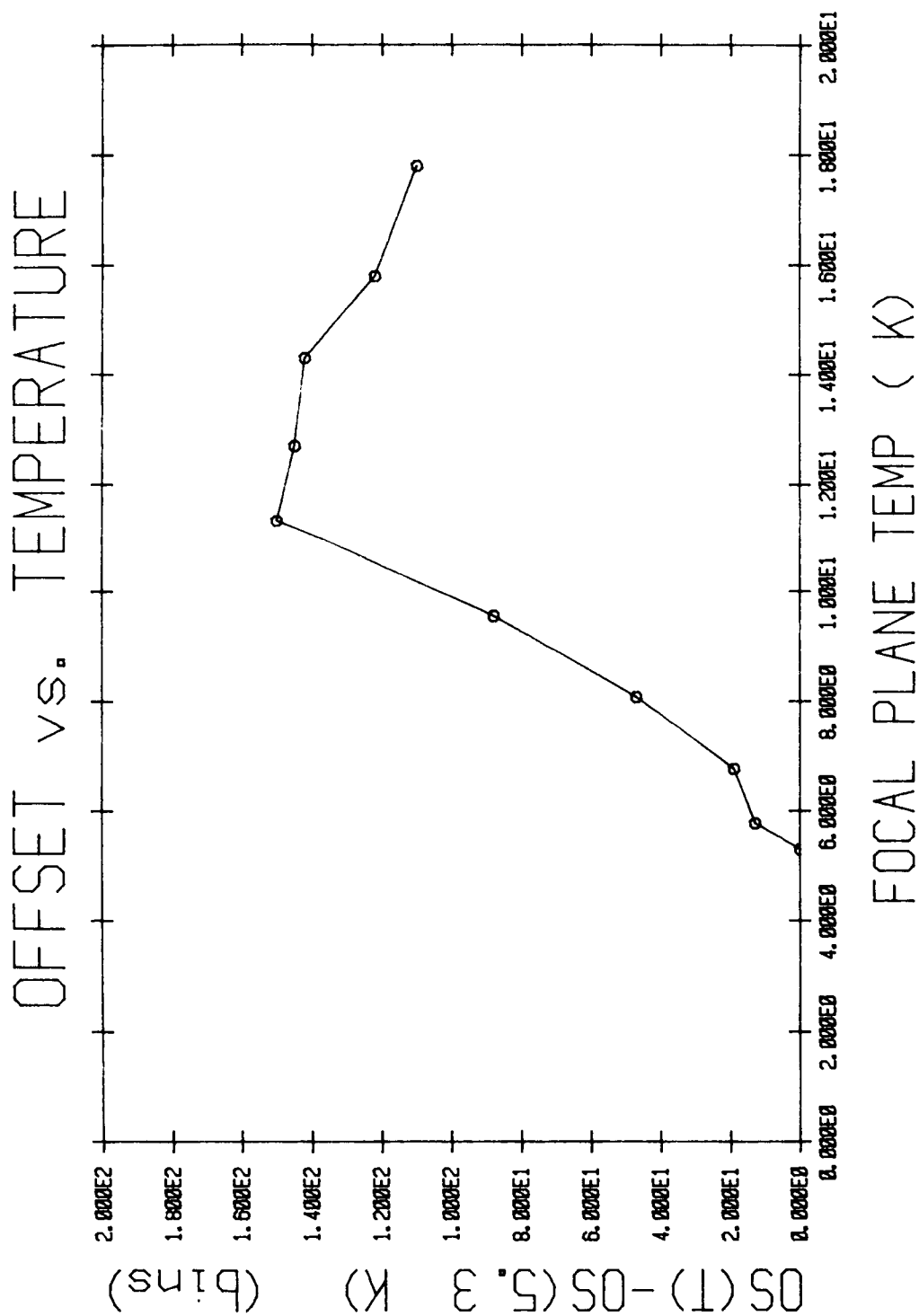


Figure 30. Relative Offset vs. Focal Plane Temperature.

Pixel [4, 4]
 Bin sensitivity Sb = 182 e/bin
 Integration Time t = 10.24 sec
 Net Detector Bias E = 0 volts
 Error ± 1 bin

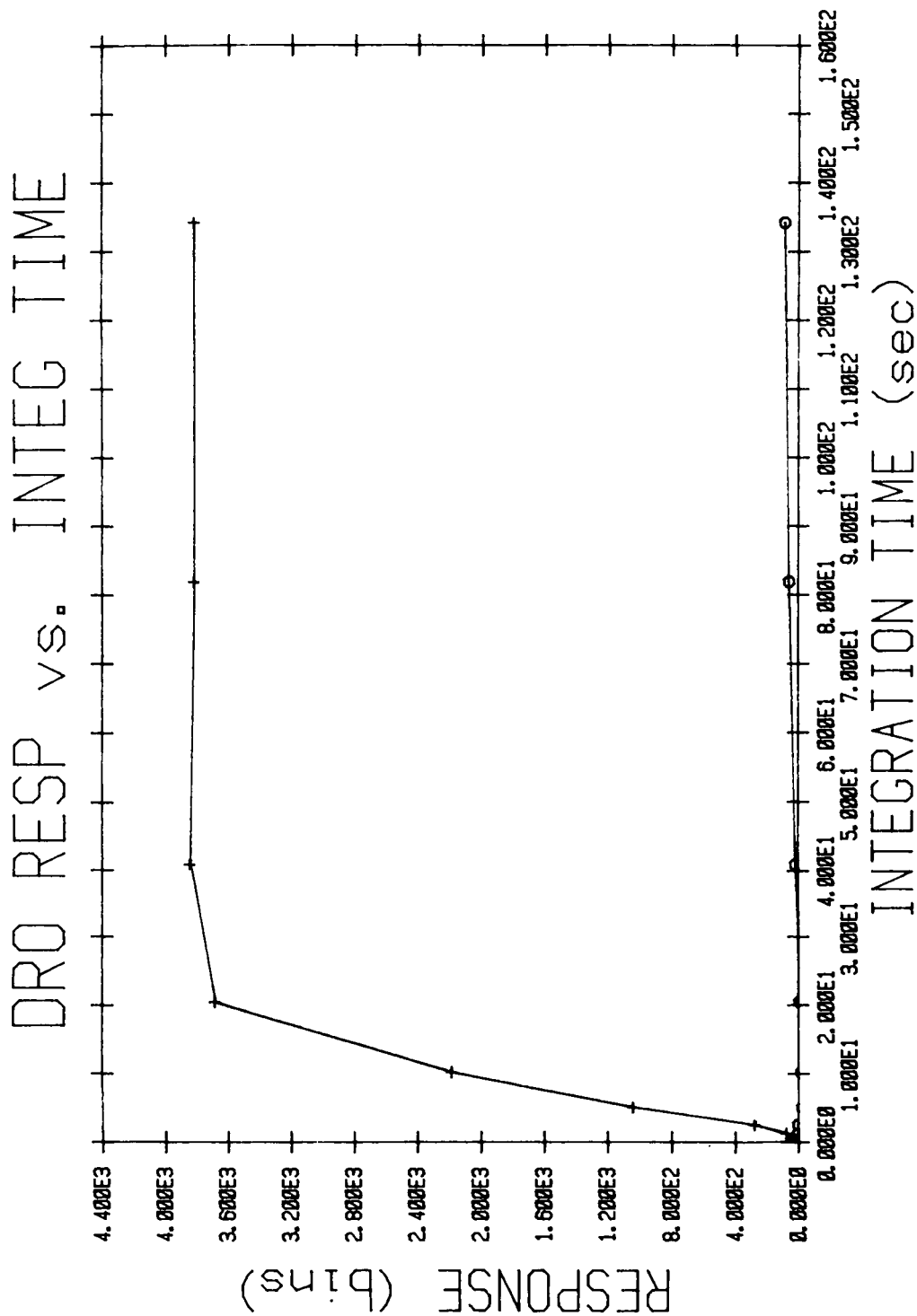


Figure 31. DRO Response vs. Integration Time.

Pixel [4, 4]
 Bin sensitivity Sb = 182 e/bin
 Focal Plane Temperature 5.4 K
 ° Dark Current Net Detector Bias E = 10 volts
 + Photo Response Net Detector Bias E = 10 volts

ORIGINAL PAGE IS
OF POOR QUALITY



Figure 32. Dark Current Histogram.

Range 0 to 1000 in 50 bin steps for 134 sec integrations
7% in Peak
Mean 318 e/s Standard Deviation 176 e/s
No gain correction
Pixel [4, 4] Dashed Line

7

HISTOGRAM

DR0:cdds = 1

Frame #: 60

Coads : 1

mean : 3.1802e+02

st dev : 1.7636e+02

samples: 256

high : 0

low : 0

BINS : 100

COUNTS (%)

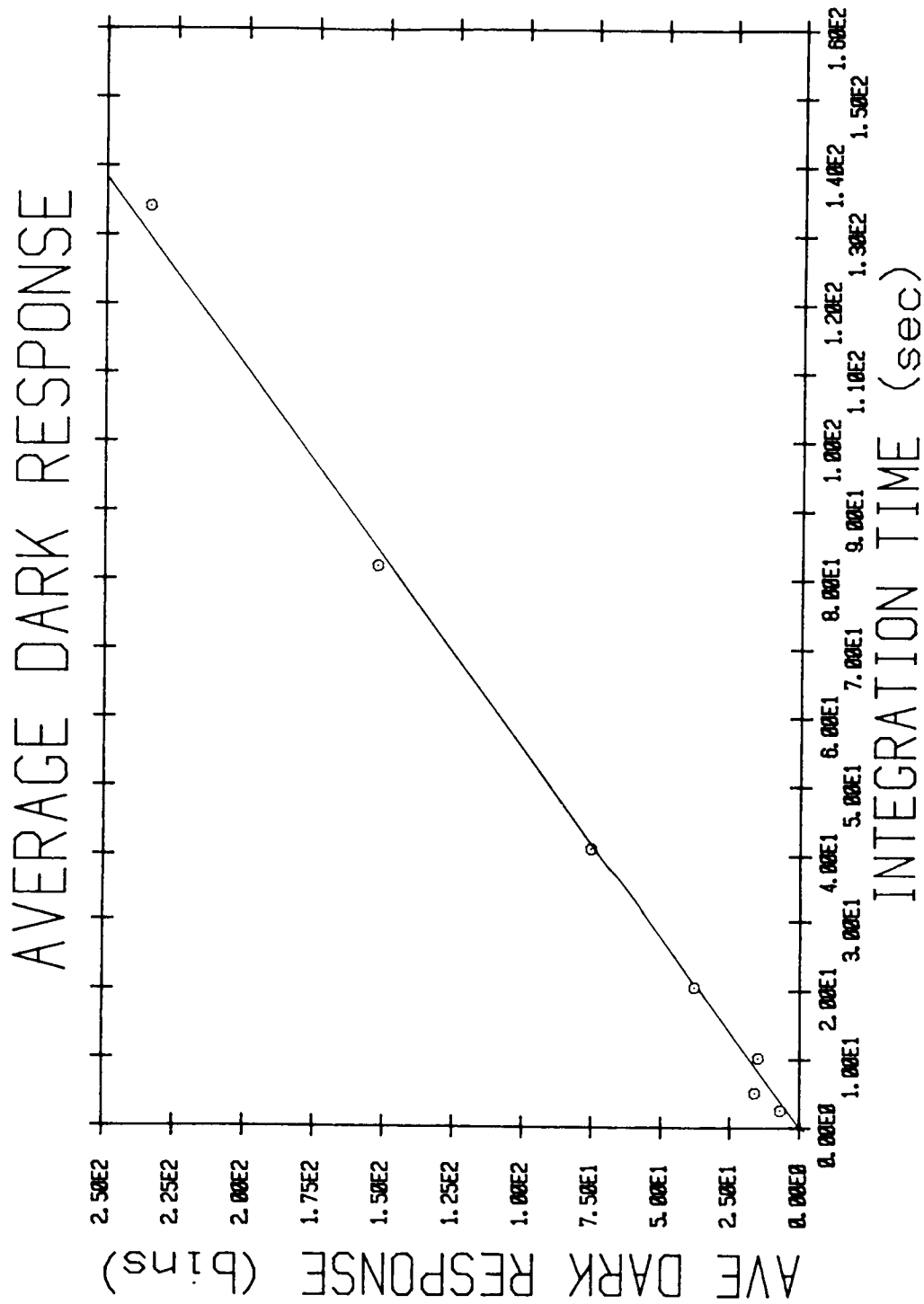


Figure 33. Average Array Dark Response.

16 x 16 subarray average
 Bin sensitivity $S_b = 182 \text{ e/bin}$
 Focal Plane Temperature 5.4 K
 Net Detector Bias $E = 10 \text{ volts}$

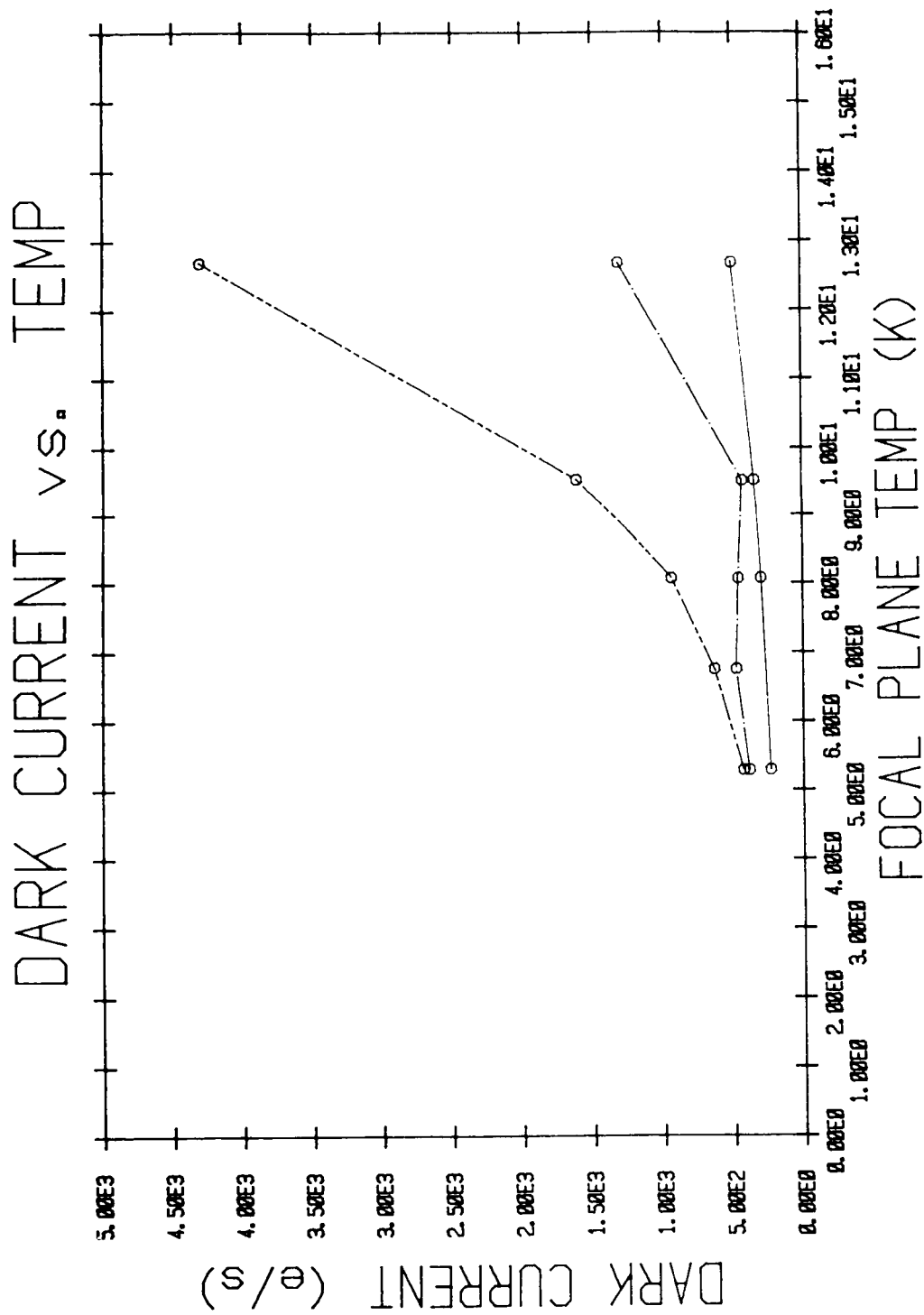


Figure 34. Dark Current vs. Temperature.

Pixel [4, 4] (line, [8, 2] (double dot dash), [12, 7] (dot dash)

Bin sensitivity $S_b = 182 \text{ e/bin}$

Integration Time $t = 134 \text{ sec}$

Net Detector Bias $E = 10 \text{ volts}$

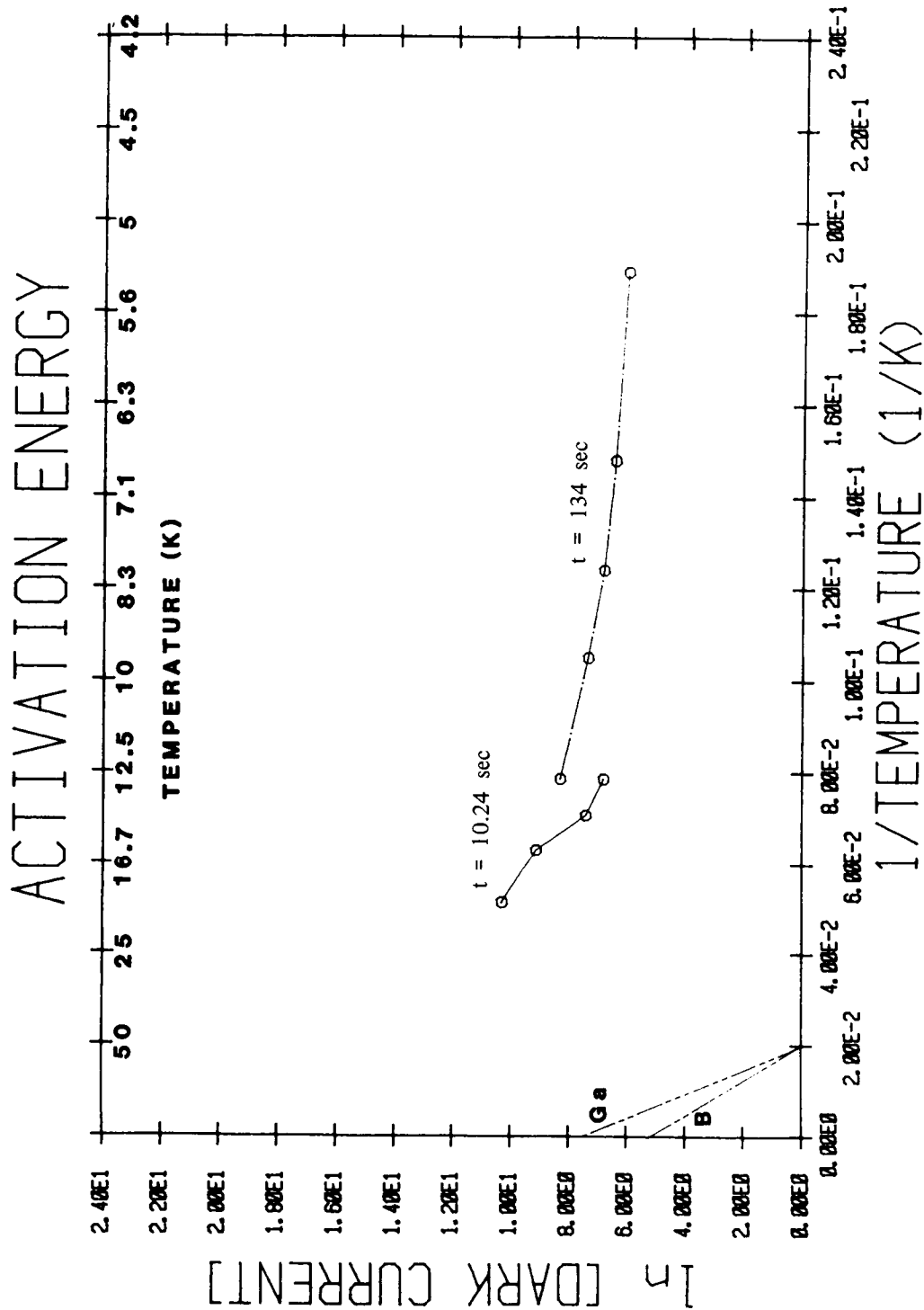


Figure 35. Activation Energy of Pixel [8, 2] Dark Current.

Bin sensitivity $S_b = 182$ e/bin
 Integration Time $t = 134$ sec (dot-dash); 10.24 sec (line)
 Net Detector Bias $E = 10$ volts
 Slope for Gallium and Boron indicated

IMAGING

The program to evaluate the imaging properties of the DRO array under SIRTf operating conditions was recently initiated. The purpose of this activity was to conduct a preliminary imaging test to determine the background, background subtraction requirements, flat field requirements, spatial crosstalk, and the spatial resolution.

The test dewar was modified to include cold imaging optics, cold filter, neutral density filters, and cold stops (Figure 36). The optic cell was composed of a field stop, a field lens, a Lyot stop, and a relay lens (1). This arrangement provided control of the magnification, system throughput and cold baffling. The lenses provided a 1.5 X magnification of the pixels at the field stop. The lenses were anti-reflection coated germanium with a peak transmission at 10 micrometers. The cold filter was centered at 11.9 micrometers and had a .12 micrometer bandwidth. A filter wheel containing neutral density filters was used to attenuate the signal and background.

The timing generator was programmed to read out half of the array (29 X 62). At the maximum readout rate for the IRAC band II test system the minimum integration time per frame was 0.5 sec.

An external black body source was imaged onto the array through the dewar. The optics used provided for controlled throughput, background minimization, and known magnification. The spectral range was set by a cold infrared filter with peak at 11.9 micrometers and a bandwidth of .12 micrometers. The room temperature background, with a 10% neutral density filter, was 2×10^7 photons/sec per pixel.

The image procedure was as follows: an image was taken of the background while looking at an aluminum plate; next an image of the apertured black body was taken; finally, the two images were differenced and then displayed.

The results of background subtraction for target apertures from 0.06 to 0.5 cm are seen in Figures 37 through 40. The array image symmetry is excellent. Note in Figure 37 the image y-centroid is centered on a pixel with equal pixels above and below with identical color. The image x-centroid is aligned with a pixel edge and the colors are weighted accordingly.

A flat field was generated by imaging the cold stop and a paper card at room temperature through a .1% neutral density filter. The images were differenced and normalized to the reference pixel [4, 4]. The repeatability and sensitivity of the flat field for the DRO are currently under investigation. However, the feasibility of flat field gain correction to the 3% level appear entirely feasible.

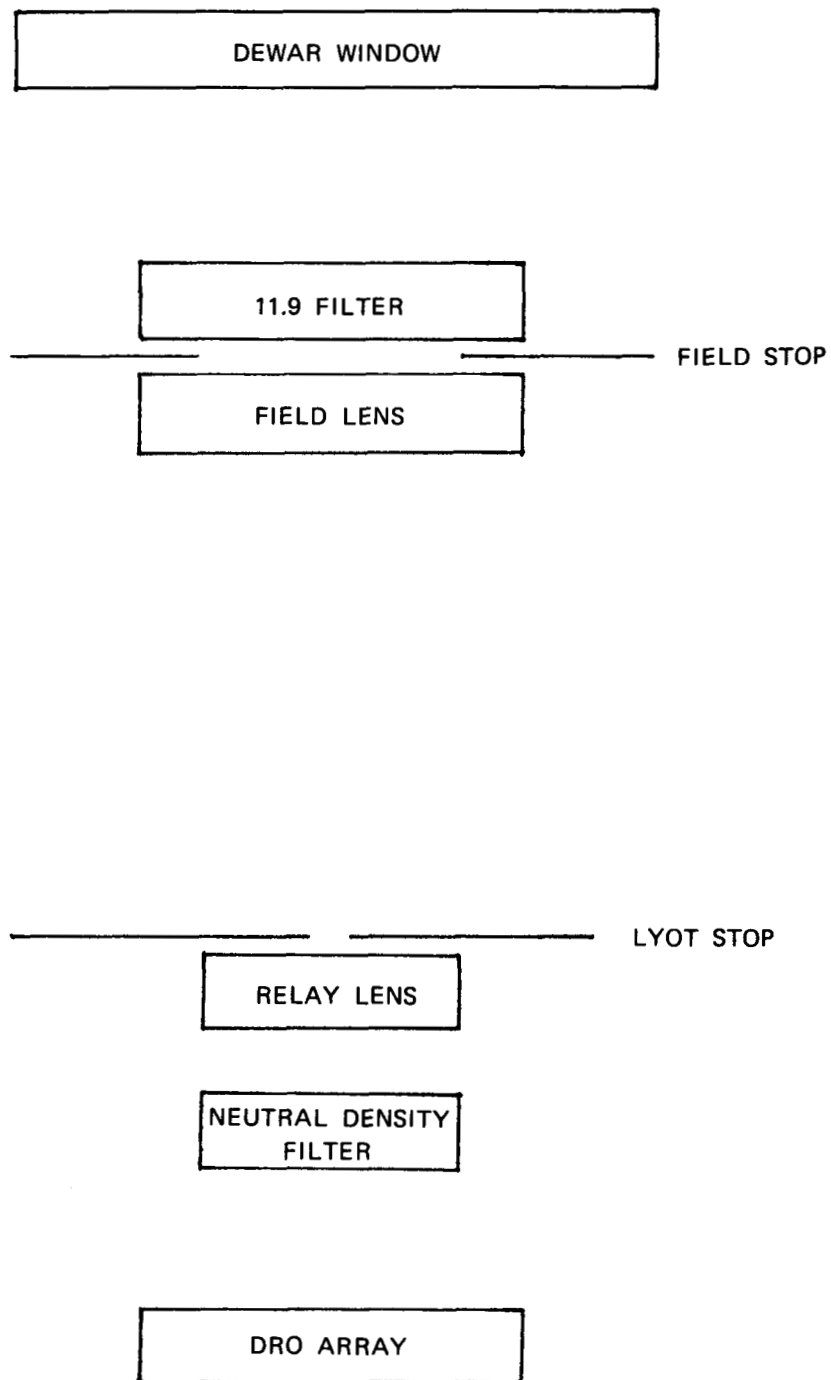


Figure 36. Image Test Set Up.

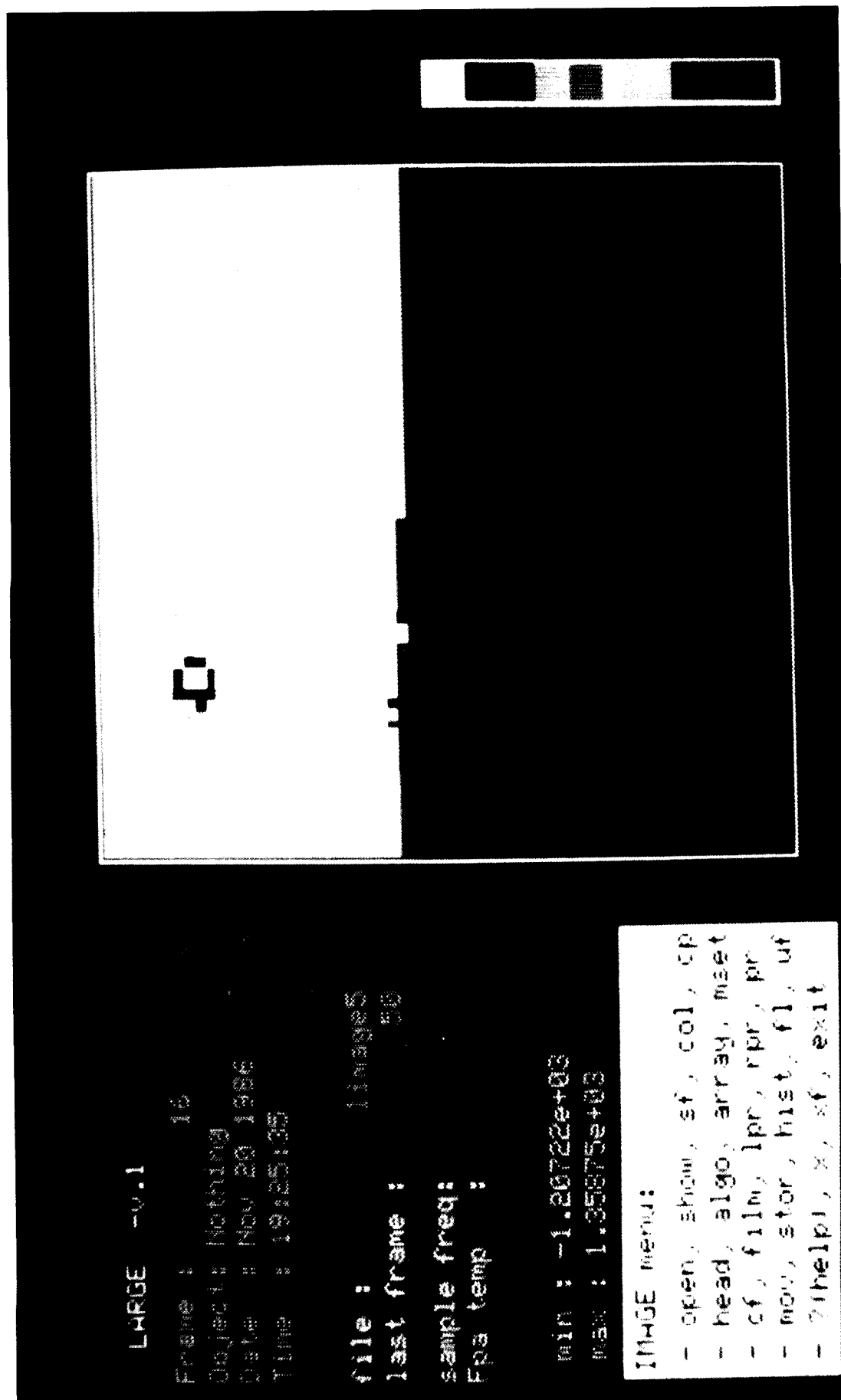


Figure 37. Images of Spot Target.
Image Diameter 0.0635 cm

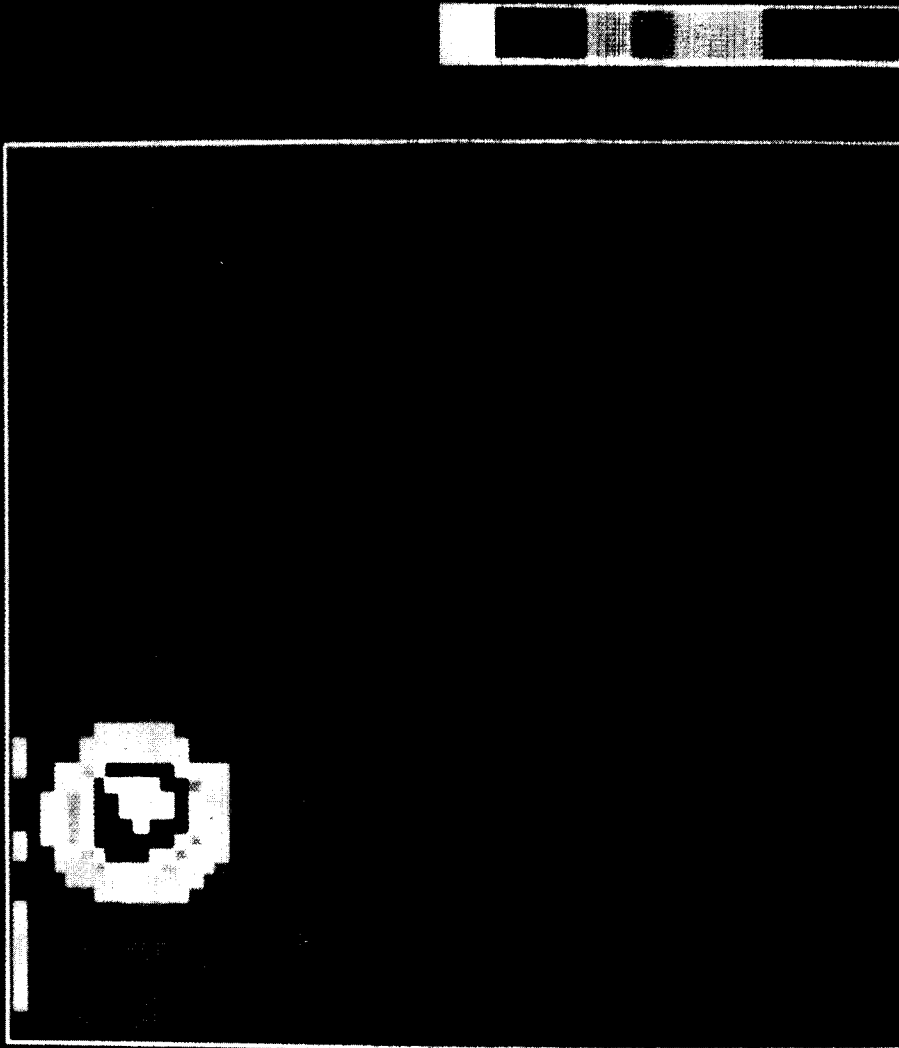


image : 1

Object: nothing
Date: 10/10/1999
Time: 14:23:33

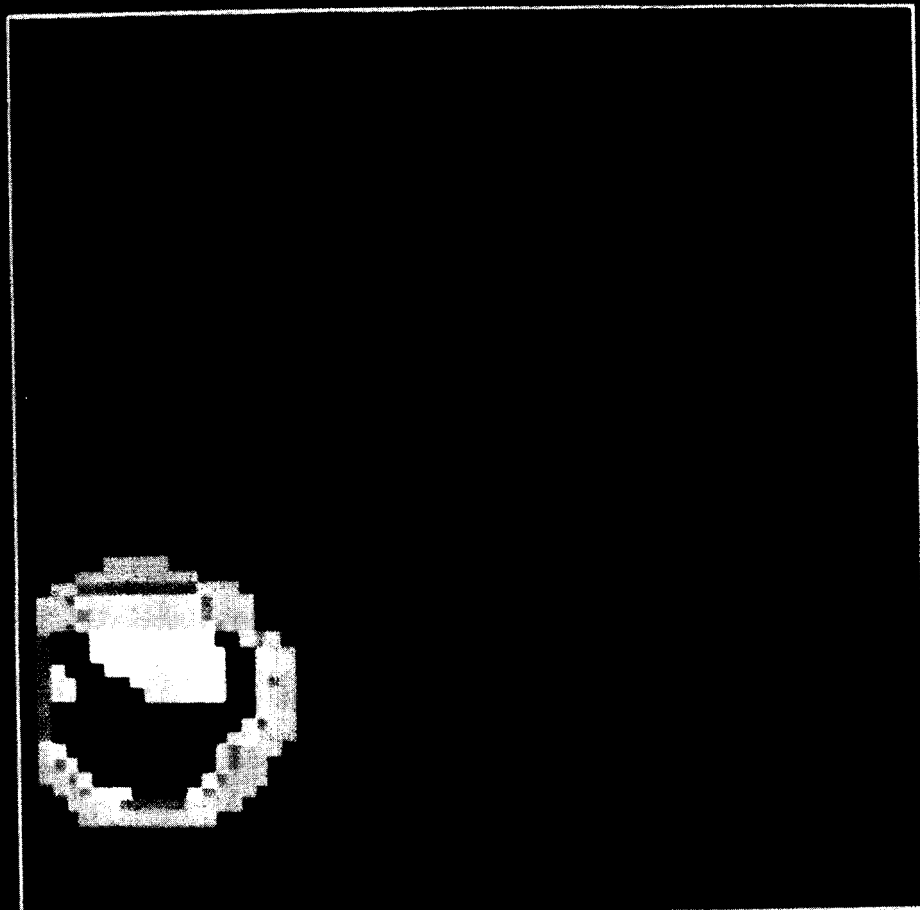
file : images
last frame : 1
sample freq:
Epa temp :

min : -1.05666e+03
max : 2.5579e+03

IMAGE menu:

- open, show, sf, col, cp
- head, algo, array, mset
- cf, film, lpr, rpr, pr
- mov, stor, hist, fl, uf
- ?help, x, sf, exit

Figure 38. Images of Spot Target.
Image Diameter 0.127 cm

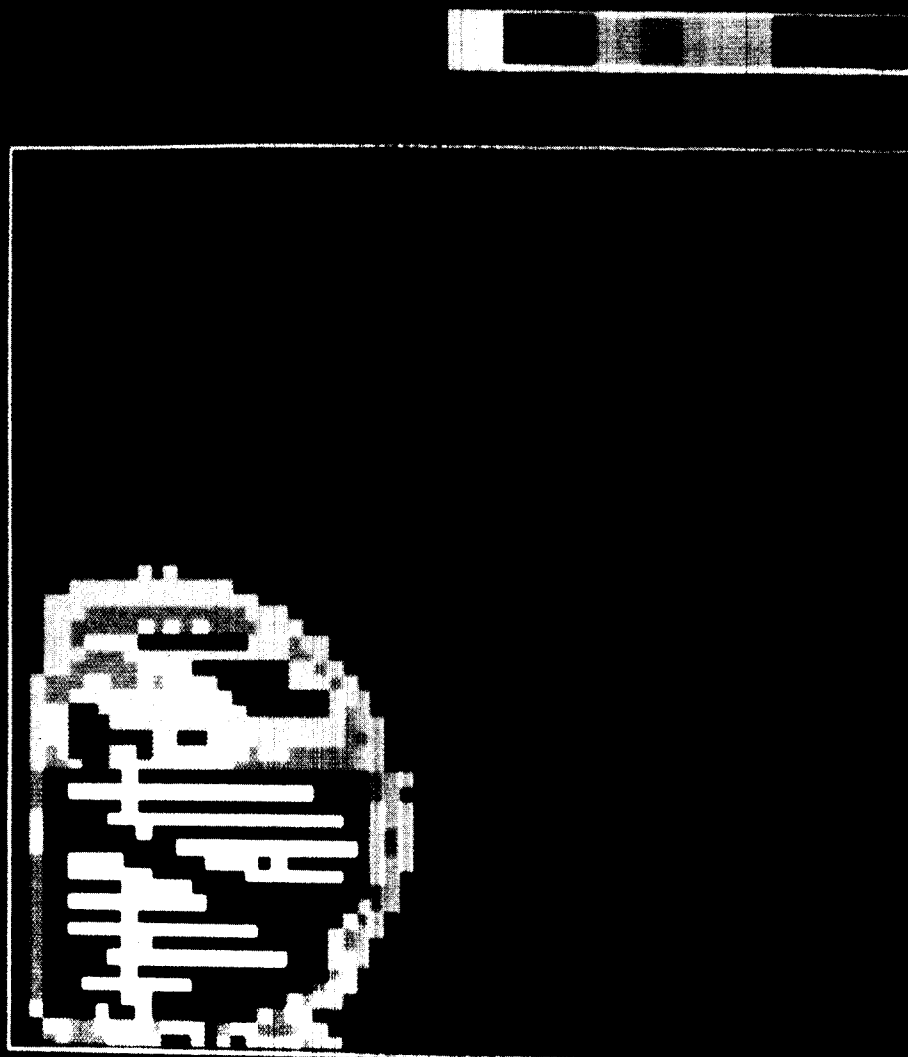


file :
last frame :
sample freq:
Fpa temp :

min : -9.23863e+02
max : 3.41100e+03

IMAGE menu:
- open, show, af, col, cp
- head, algo, array, mset
- cf, filon, lpr, rpr, pr
- mov, aton, bist, fl, ut
- (help) on, f, e, s, t

Figure 39. Images of Spot Target.
Image Diameter 0.254 cm



```

Frame 1
Object: Spotting
Date: 10/20/88
Time: 13:05:08

```

```

file:
last frame:
sample front:
Epa temp:

```

```

min: -3.24750e+02
max: 3.53722e+03

```

IMAGE menu:

- open, show, sf, col, cp
- head, algo, array, mset
- cf, film, lpr, rpr, pr
- mov, stor, hist, fl, uf
- ?(help), x, xf, exit

Figure 40. Images of Spot Target.
Image Diameter 0.508 cm

CONCLUSIONS

The performance summary to date for the CRC 228 Si:Ga array is summarized in Table 6.

Table 6. Si:Ga CRC 228 Performance Summary at 5.4 K.

Read Noise	255 e rms best	424 e rms worst
Dark Current	318 \pm 176 e/s	worst case
Responsivity (9)	4.7 A/W	
Power Dissipation	2.51 mW @ 70 f/s	

The best case measured read noise for the DRO array is in excess of the expected DRO MOSFET limited read noise of 49 e rms (Table 5). In an effort to understand the dominant effects contributing to the excess read noise, the analog processor parameters and array noise sources were investigated in a simplified system model.

The change in predicted read noise using the DRO MOSFET noise model described above as a function of excess $1/f$ noise is shown in Figure 41. If the excess is entirely due to $1/f$ noise, this would imply a source with an equivalent input spectral density of 11.3 microvolt/ $\sqrt{\text{Hz}}$ @ 10 Hz. If entirely due to broadband white noise, the observed excess would imply a source with an equivalent input spectral density of 318 nv/ $\sqrt{\text{Hz}}$ in the 220 kHz warm preamplifier bandwidth (Figure 42). The possibility of several excess noise sources with both $1/f$ and broadband components can not be ruled out. The source of the excess noise is under investigation.

A method for analyzing the infrared array detector dark current separately for each pixel has been demonstrated. The dark current of pixels in the main body of the dark current histogram as well as pixels with local excess dark current can be further analyzed to determine the activation energy of the impurity or impurity complex contributing to the dark current.

Based on the 16 x 16 subset tested the worst case upper limit on the dark current for this particular array, at a focal plane temperature of 5.4 K, is 318 e/s \pm 177 e/s. The dark current can in general be lowered by decreasing the concentration of the detector impurity causing the dark current or lowering the detector operating temperature. However, in reducing the operating temperature a conflict arises. By extrapolating the read noise to lower temperatures (Figure 25) one would predict a degraded read noise. Also, some reduction in the responsivity of the device is observed as the temperature is lowered. These effects will have a direct impact on the device NEP and favor the reduction in the impurity causing the dark current.

The power dissipation at the cold surface for the array tested was less than 3 mW including power dissipated in the array output driver source resistors and in the input protection circuitry. The operation of a device similar to the CRC 228 for the SIRTf/IRAC instrument would appear entirely feasible with a 3 mW budget.

The performance of this Si:Ga DRO has been measured under SIRTf simulated conditions on the Goddard Space Flight Center detector test system. Worst case measurements for the performance have been established (Table 6). Analysis supporting the measurement program has been conducted. Areas for improvement have been highlighted. The performance of this device is very good compared to previous devices tested (4). The effects of the test system on the read noise, and dewar light leakage on the dark current, have not been entirely removed so only upper boundaries on the performance are established.

The next phase in the program includes the implementation of the improvements identified in this phase and continued imaging with the array. To establish the device to device performance variation and an anticipated yield for these types of arrays, the evaluation of additional Band II array devices is also planned.

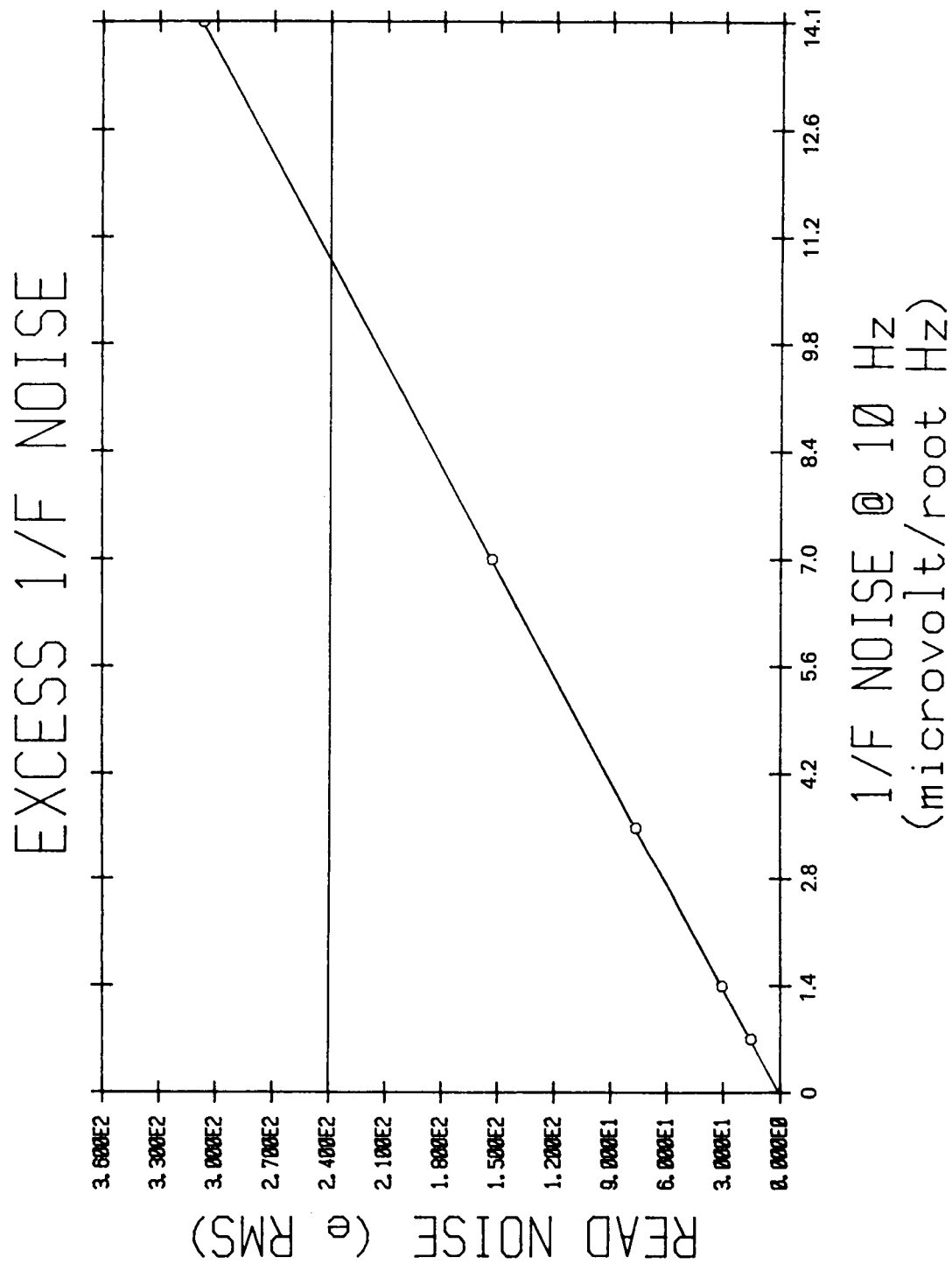


Figure 41. Theoretical Read Noise vs. 1/F Noise.

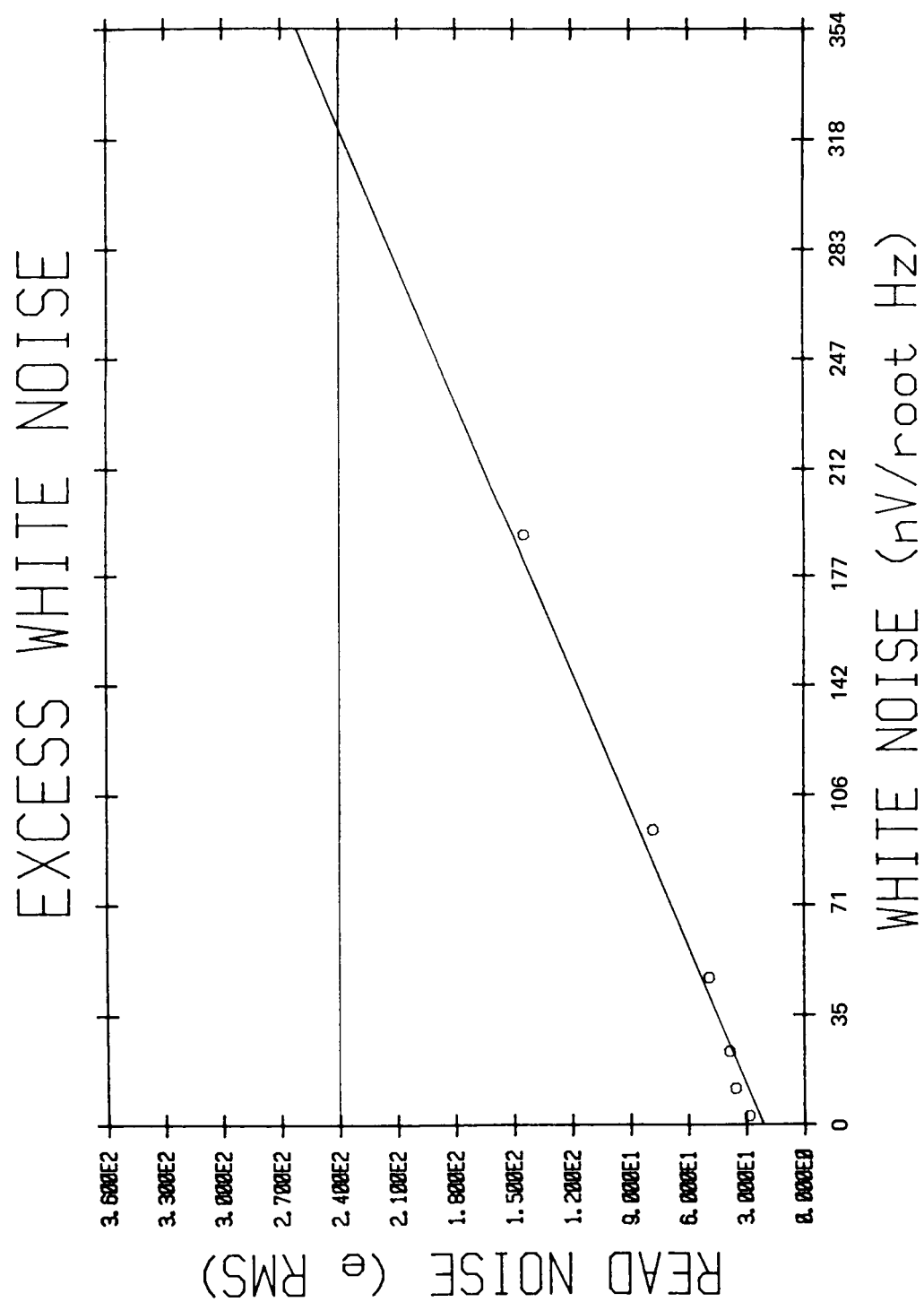


Figure 42. Theoretical Read Noise vs. White Noise.

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15. Supplementary Notes Jeff Bowser; STX Corporation; Lanham, Maryland, 20706					
16. Abstract A direct readout (DRO) infrared detector array, a candidate for the Space Infrared Telescope Facility (SIRTF) Infrared Array Camera (IRAC), has been tested with a readout system built at the Goddard Space Flight Center. The array, developed by Santa Barbara Research Corporation (SBRC) for different applications, has a detector surface of gallium doped silicon, bump bonded to a 58 X 62 pixel MOSFET multiplexer on a separate chip. Although this chip and system do not meet all the SIRTf requirements, the critically important read noise is within a factor of 3 of the requirement. Significant accomplishments of this study include: 1. Development of a low noise correlated-double-sampling readout system with a readout noise of 127 to 164 electrons, (based on the detector integrator capacitance of 0.1 pF), 2. Measurement of the readout noise of the detector itself, ranging from 123 to 214 electrons with bias only (best to worst pixel), and 256 to 424 electrons with full clocking in normal operation, at 5.4 K where dark current is small; 30% smaller read noises are obtained at a temperature of 15 K;* 3. Measurement of the detector response versus integration time, showing significant nonlinear behavior for large signals, well below the saturation level, 4. Development of a custom computer interface and suitable software for collection, analysis, and display of the detector data. A number of areas for additional work remain.					
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